SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

TV EAST/WEST CORRECTION CIRCUITS

SUMMARY **Page**

SUMMARY (continued)

I - TV EAST/WEST CORRECTION GENERAL PRINCIPLES

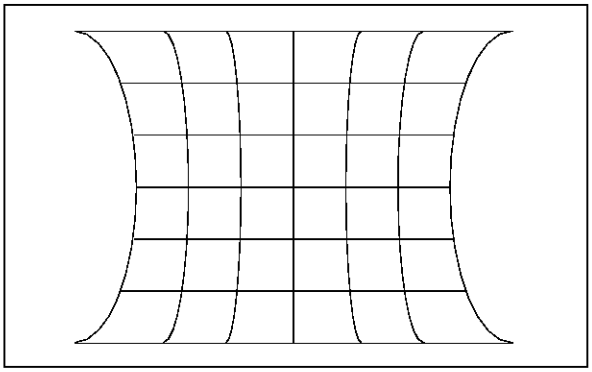
I.1 - INTRODUCTION

All color picture tubes which are used in the present TV-sets have a magnetic deflection system. Using a homogenous magnetic field, we have generally a pillow-distortion of a rectangular picture on the screen. This is mainly due to the tangens relation between the deflection angle and the beam position on the screen

Using a well dimensioned and optimized inhomogenous magnetic deflection field, this distortion can be eliminated completely for picture tubes with a deflection angle of 90^o. In the same way the pillow-distortion of 110^o deflection tubes can be eliminated in the vertical direction (North-South direction). But until now the distortion in the horizontal direction (East-West direction) can not eliminated with special designed deflection yokes. A distortion remains in Figure 1.

In order to compensate this effect, the horizontal deflection current in the yoke must be modulated. This means a large amplitude of the deflection current in the middle of the screen and a small amplitude on the top and the bottom of the screen. The general behaviour of the deflection currents is illustrated in Figure 2.

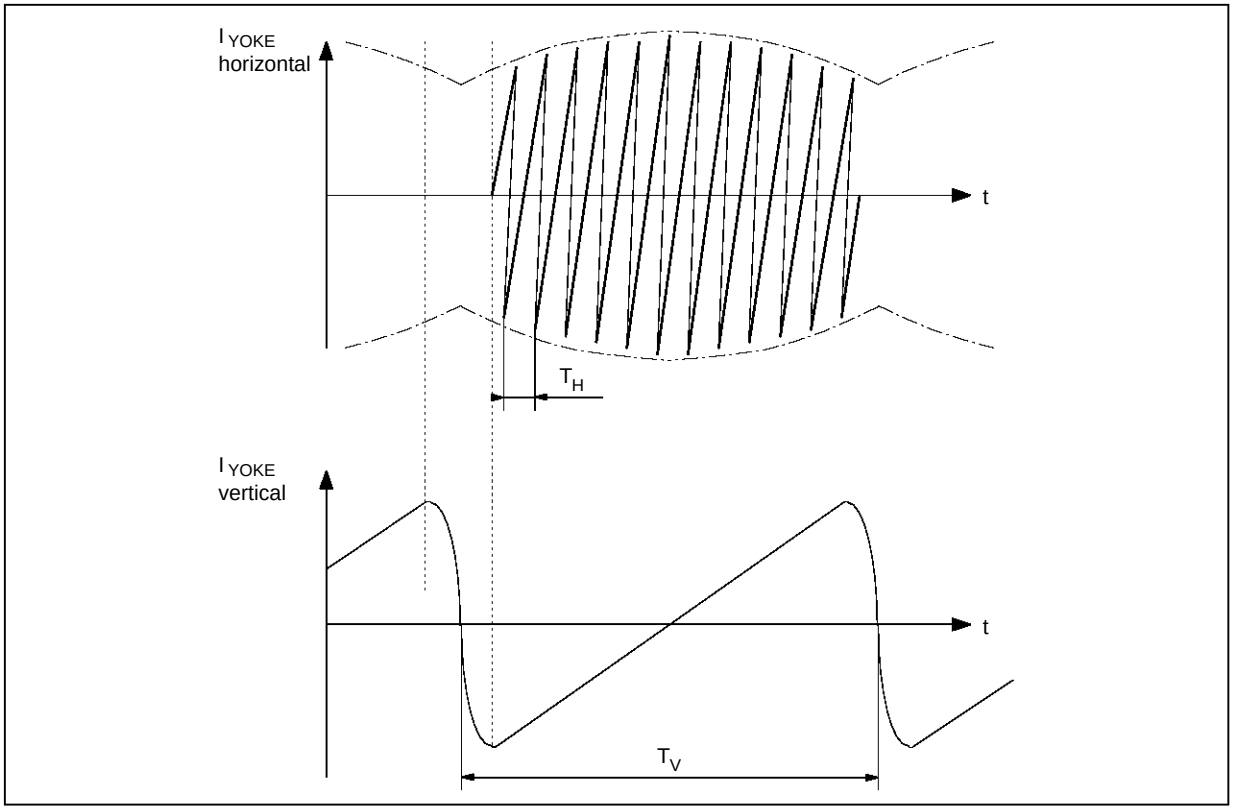
Figure 1 : Test Grid on a 110^o Color Tube



In this picture T_V and T_H are the time periods for the vertical and the horizontal deflection. Note that the envelope of the horizontal yoke current must be a parabola with the same phase as the vertical saw-tooth current. This means an East/West correction can be reached by modulating the horizontal yoke current with a parabola.

There are different possibilities to modulate the yoke current. The most convenient modulator is the so-called **Diode Modulator** described in the next chapter.

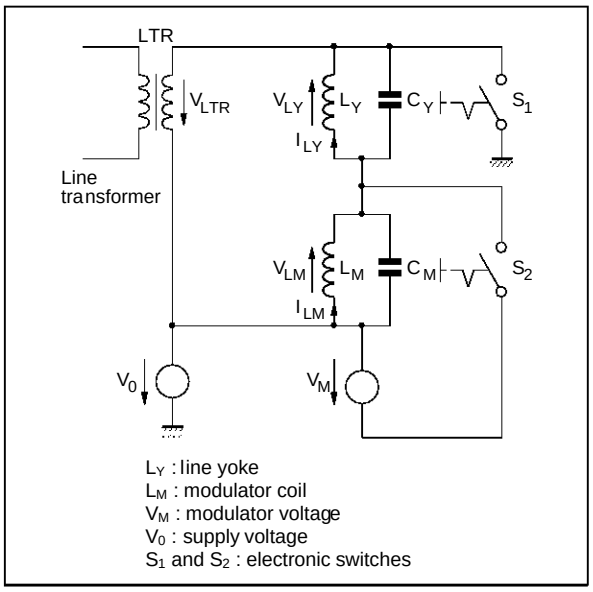
Figure 2 : Horizontal and Vertical Yoke Current (T_H = 64µs, T_V = 20ms)



I.2 - DIODE MODULATOR PRINCIPLE

Let us consider the basic circuit of the horizontal deflection unit as shown in Figure 3.

Figure 3 : Basic Circuit of the Horizontal Deflection Power Stage including Modulator



For the sake of simplicity, the electronic switches (diodes and transistors) are drawn as simple switches S_1 and S_2. The deflection time T_H of 64µs can be divided in two parts : the scan time T_S at which the electronic switches S_1 and S_2 are closed and the flyback time T_F (S_1 and S_2 opened). The total time period is the

$$T_H = T_F + T_S \quad (1.1)$$

We assume now that the line transformer L_{TR} have a neglectable high inductance and the time behaviour is mainly determined by L_Y, L_M, C_Y, C_M. Small modifications are necessary to consider also the electrical characteristics of L_{TR}, but they should not be discussed here.

During the scan time the inductors L_Y and L_M are directly connected to the voltage sources V_0 and V_M :

$$\left.\begin{array}{l} V_{LY} = V_0 - V_M \\ V_{LM} = V_M \end{array}\right\} \quad S_1 \text{ and } S_2 \text{ closed (scan time)} \quad (1.2)\ (1.3)$$

Neglecting any power consumption in possible series resistors, the current in the two inductors increases linear in time :

$$i_{LY} = \frac{t\,(V_0 - V_M)}{L_Y} \quad (1.4)$$

$$i_{LM} = \frac{t\,V_M}{L_M} \quad (1.5)$$

Since the current i_{LY} and i_{LM} must be zero-symmetrical (average value = 0), the peak value of i_{LY} and i_{LM} is obtained after half of the scan time $T_S/2$

$$\hat{i}_{LY} = \frac{T_S\,(V_0 - V_M)}{2\,L_Y} \quad (1.6)$$

$$\hat{i}_{LM} = \frac{T_S\,V_M}{2\,L_M} \quad (1.7)$$

After this time, S_1 and S_2 are opened and the energy in the inductors L_Y and L_M changes to the capacitors C_Y and C_M. We assume now the same resonance frequency for both LC parts

(1.8)

$$L_Y\,C_Y = L_M\,C_M = L\,C \quad (1.8)$$

Under this condition, both capacitors C_Y and C_M have its peak voltage at the half of the flyback time $T_F/2$. The energy in the inductors stored at the end of the scan period

$$E_L = \frac{1}{2}\,L\,(i_L)^2 \quad \text{is then} \quad (1.9)$$

completely transformed into the capacitor

$$E_C = \frac{1}{2}\,C\,(V_C)^2 \quad (1.10)$$

Under this condition, we obtain the general equation for the peak voltage in the middle of the flyback period

$$\hat{V}_C = -\,\hat{i}_L\,\sqrt{\frac{L}{C}} + V_{init} \quad (1.11)$$

This voltage is the addition of the initial voltage and the voltage increase due to the energy transfer. With (1.6) and (1.11) we get

$$\hat{V}_{LY} = \hat{V}_{CY} = -\,\frac{V_0 - V_M}{\sqrt{L_Y\,C_Y}}\,\frac{T_S}{2} + (V_0 - V_M)$$

$$= (V_0 - V_M)\,(1 - \frac{T_S}{2\sqrt{L\,C}}) \quad (1.12)$$

in the same way (1.7 and 1.11) we obtain

$$\hat{V}_{LM} = \hat{V}_{CM} = V_M\,(1 - \frac{T_S}{2\sqrt{L\,C}}) \quad (1.13)$$

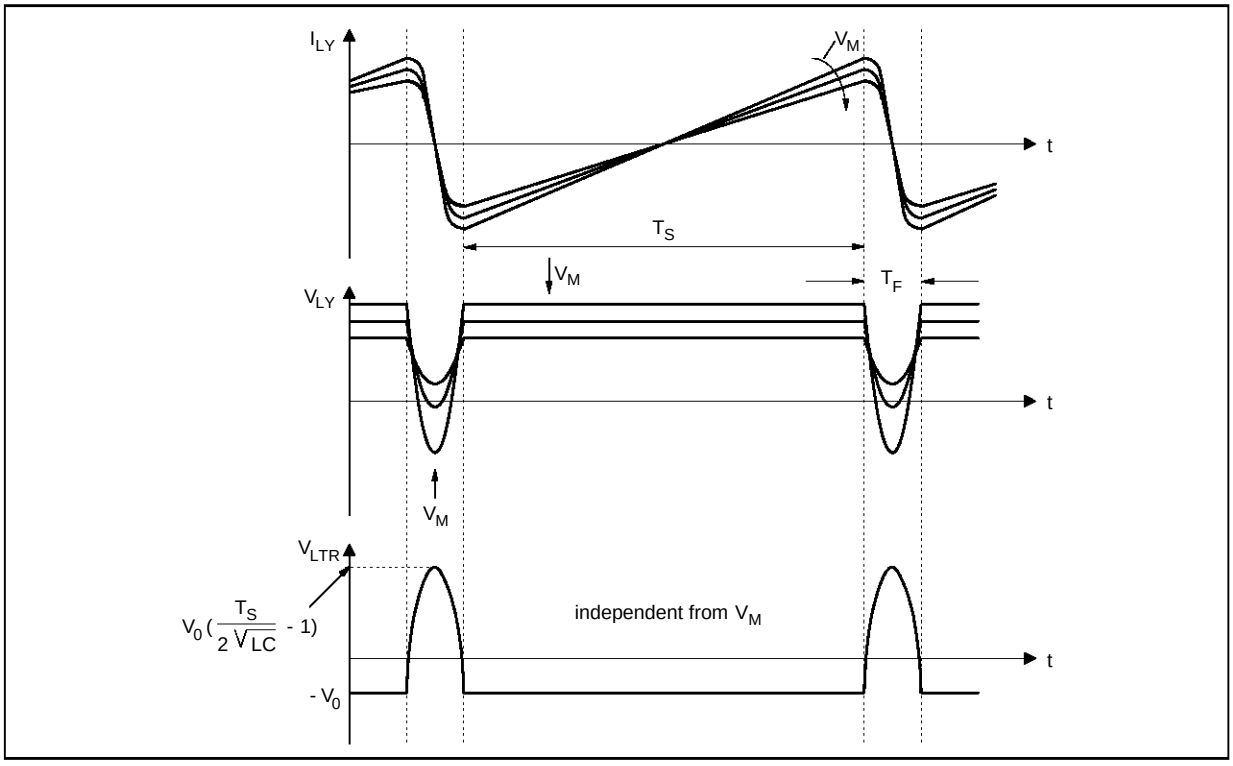
The resulting peak voltage during the flyback time at the line transformer is then

$$\hat{V}_{LTR} = -\,\hat{V}_{LY} - \hat{V}_{LM} = V_0\,(\frac{T_S}{2\sqrt{L\,C}} - 1) \quad (1.14)$$

Please note that in this circuit, the horizontal flyback voltage V_{LTR} (1.14) is independent from the modulation voltage V_M, though the yoke current I_{LY} can be changed via the modulator voltage V_M (see 1.6)

An overview of the currents and voltages is given in Figure 4.

Figure 4 : Currents and Voltages of the Basic Circuit



For a practical application, a large capacitor C_S can be inserted in series to the yoke to get an S-correction of the deflection current I_{LY}. Simultaneously, the voltage V_M can be grouded to have a simpler handling of the modulator driver. The switch S_1 is a standard high voltage power transistor (e.g. BU508A or S2000AFI), the switch S_2 can be replaced by 2 diodes as shown in Figure 5.
Normally, the current I_M into the modulator voltage source is positive and V_M must only be realized as a variable resistor (e.g. transistor T_M).
Many manufacturers use this simple diode modulator with such active load. A disadvantage of this application is the power consumption in the power transistor T_M (~2W). Under ideal conditions, V_M should have no power consumption (average $i_M = 0$), but in practice the coils and the line transformer are not free from parasitic resistors. Furthermore a reasonably large power is used from the various loads on the line transformer.

An improvement from the power consumption point of view is the use of a switched power stage V_M. For this purpose, an additional inductance L_S (5...20mH) is used and connected as shown in Figure 6.

Point A is biased from a pulse-width modulated rectangular wave. The frequency is arbitrary, for a simple pulse-width modulator, The horizontal line frequency is used normally.

Figure 5 : Standard Diode Modulator with Class-A Modulator Driver

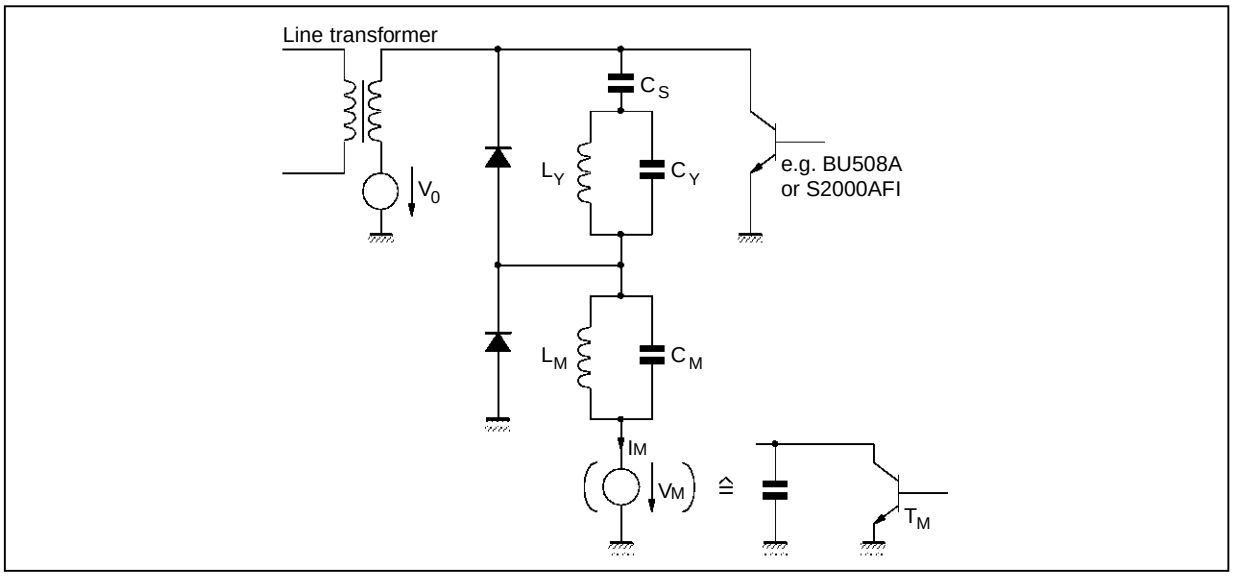
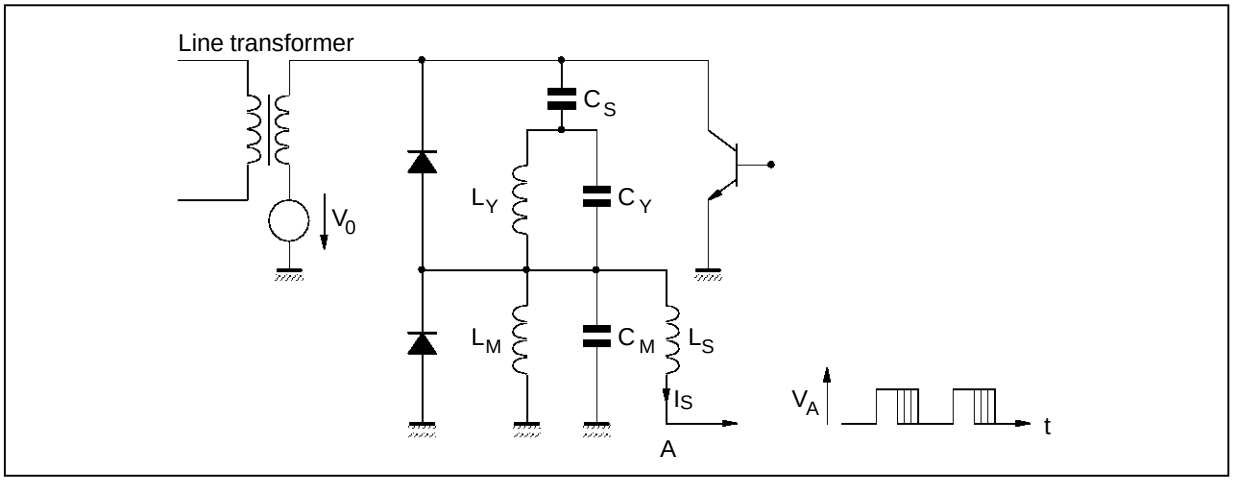


Figure 6 : Standard Diode Modulator with Class D Modulator Driver (pulse-width modulator)



I.3 - PULSE-WIDTH MODULATOR PRINCIPLE

The pulse-width modulator for driving the diode modulator contains mainly one power comparator with the external circuitry shown in Figure 7.

The working frequency is determined by the linear saw-tooth voltage biasing the positive comparator input. It is generated by the flyback pulses of the line transformer. The current sink on the positive input discharges the capacitor C_S during the scan time T_S and yields the negative slope of the saw-tooth voltage.
The negative input is biased from a parabola voltage, its generation is discussed later.

To improve the performance of this pulse-width modulator, a feedback path R_K is provided compensating variations in the power supply V_{CC} of the comparator. The capacitor C_K together with R_{in} and R_K serves as a low-pass filter to suppress the line frequency coming from the comparator output.

If the current I_S in the inductor L_S (see Figures 6 and 7) is only positive, the output stage can have a simple darlington transistor and a diode as seen in Figure 8.

If the darlington stage is switched on, the current I_S is flowing through T_A and T_B into ground. Otherwise, the diode D is conducting and I_S flows into the supply voltage.
The power, consumed normally in L_M (see Figure 5) is then redelivered into this supply voltage.

A greater flexibility in the design of the diode modulator can be reached, if the current I_S is allowed to have negative values. For this case, the comparator power stage must be realized as push-pull stage (see Figure 9).

Due to the voltage drop across the transistors and diodes, the transition from positive values I_S and negative values I_S yields a voltage step on the output as illustrated in Figure 10.

In this case the steps in the output voltage produce an additional undesired modulation of the yoke current. Then you can see some irregularities in the vertical lines of the test grid on the screen. With the aid of a reasonable large fedback factor (small R_K, small C_S, large parabola amplitude) this effect becomes neglectable.

Figure 7 : Pulse-width Modulator

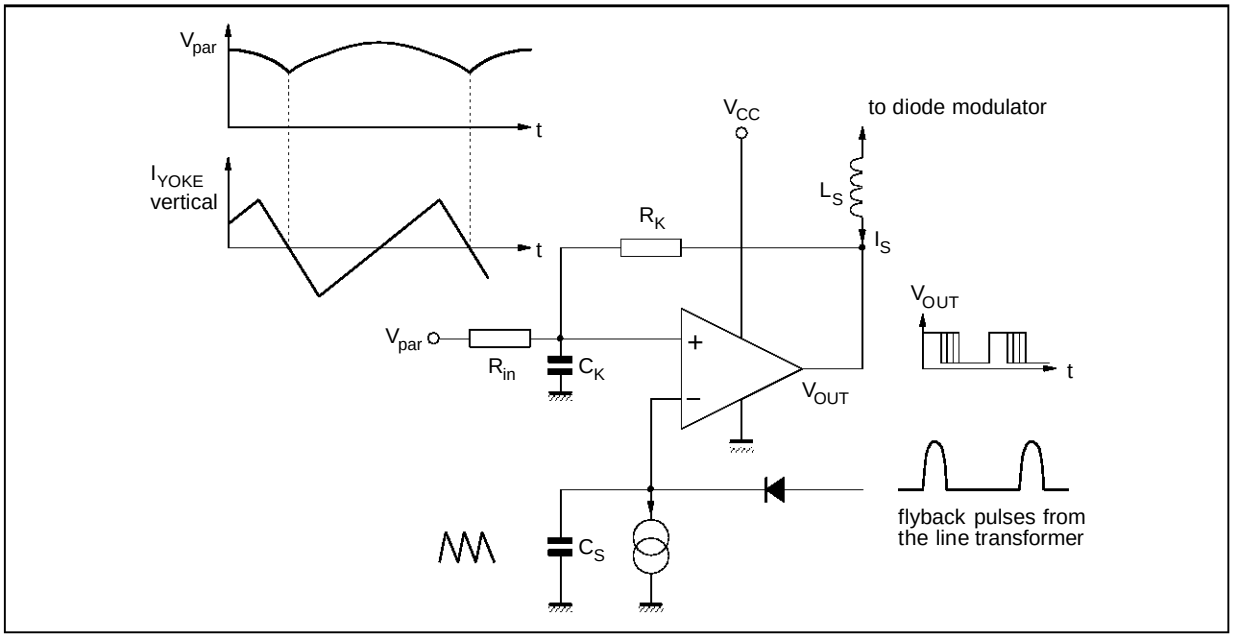


Figure 8 : Comparator Output Stage, only positive modulator current I_S is allowed

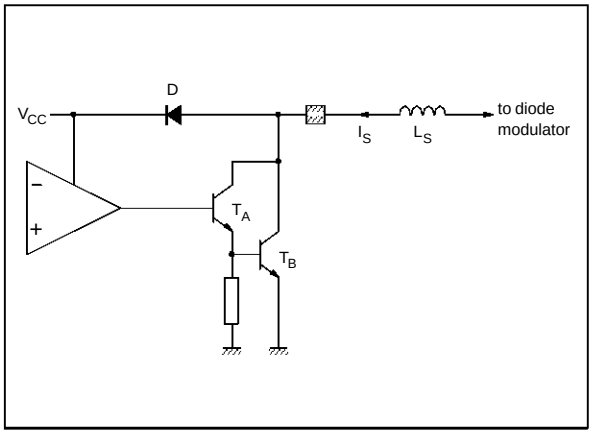


Figure 9 : Comparator Output Push-pull Stage, negative and positive modulator current I_S allowed

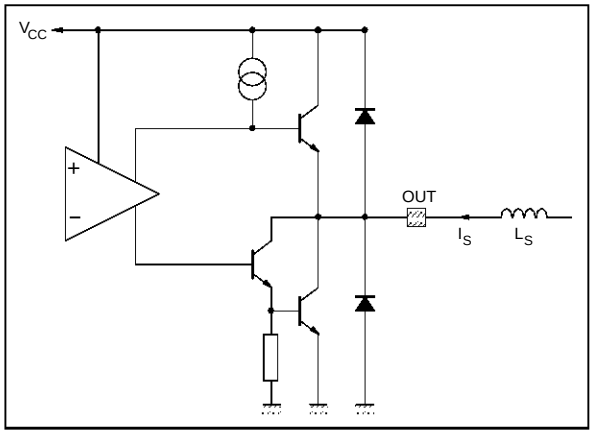
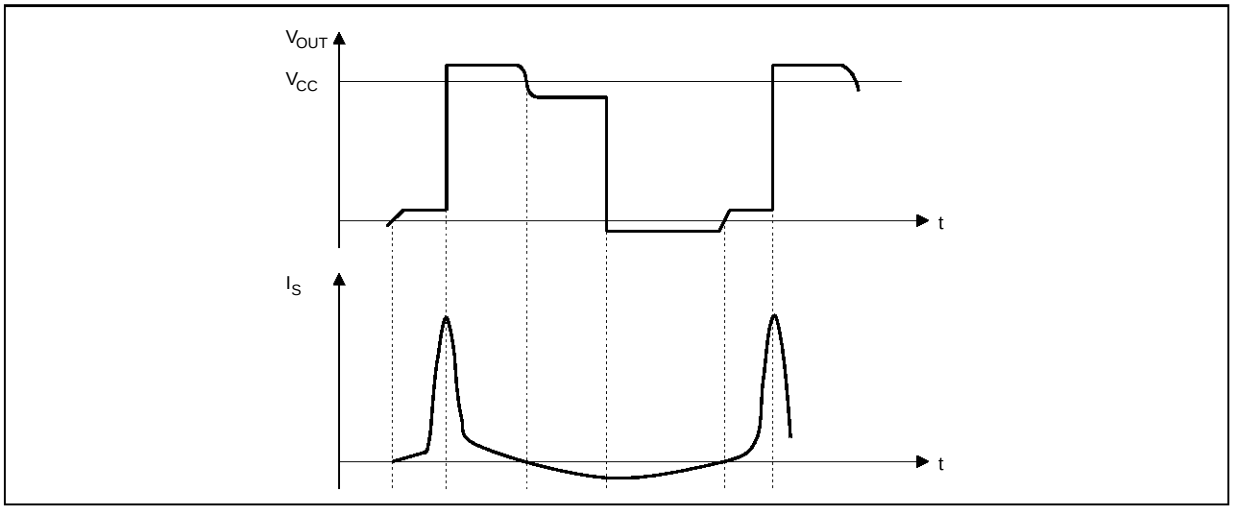


Figure 10 : Voltage on the comparator output by zero crossing of I_S



I.4 - GENERAL CONSIDERATIONS TO GENERATE THE CORRECTION PARABOLA

The correction parabola which drives the pulse-width modulator (Figure 7) must have the same frequency and phase as the vertical deflection current in the yoke. Therefore, the parabola can be generated directly from the vertical saw-tooth signal which drives the deflection output stage. Principally there are two different kinds for generating the parabola:

a) integrator-network (linear)
b) functional-network (non linear)

Let us consider first the integration method :
The vertical saw-tooth signal can be described with the following simple equation, valid for one period

$$S_{saw\text{-}tooth}(t) = A\frac{t}{T_V} \qquad 0 < t < T_V \qquad (1.15)$$

where A is the amplitude, T_V the time period and t the time.

Integrating this signal we get

$$\int_0^t S_{saw-tooth}(t)\,dt = \int_0^t A\frac{t}{T_V}\,dt = \frac{A}{2\,T_V}t^2 \qquad (1.16)$$

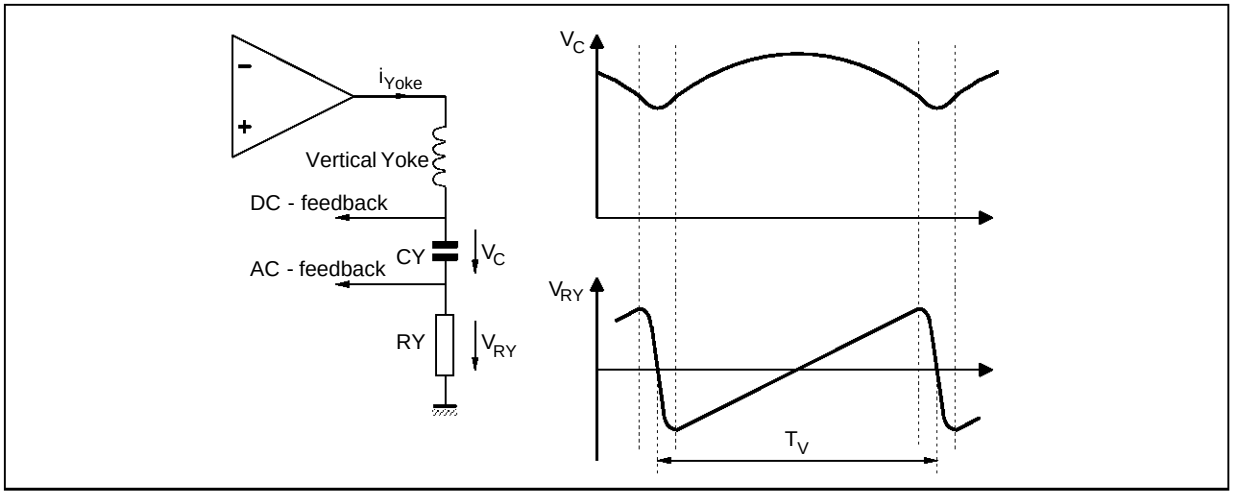
Since the relation between the current and the voltage on a capacitor is given by

$$V_C(t) = \int i_C(t)\,dt \qquad (1.17)$$

the parabola can be obtained directly from the coupling capacitor C_Y in the vertical output stage as illustrated in Figure 11.

Due to the aging and the temperature dependence of this (electrolytic) capacitor C_Y, some manufacturers prefer to generate the parabola from the voltage drop across R_Y (V_{RY}) with the aid of a separate integrator.

Figure 11 : Vertical Output Stage and Corresponding Voltages



Due to the small amount of active and passive components, this integration method is the usual method to realize the East/West correction circuit with discrete elements.

The functional network realization requires a quite larger amount of active components and is therefore especially suited for integrated circuits. The input signal for this kind of parabola generation is also the vertical saw-tooth signal corresponding to (1.15). With the aid of a functional (square) network, the square of this signal can be formed according to the following equation :

$$S_{parabola} = k\,(S_{saw-tooth} - S_0)^2$$
$$= k\,(A\,\frac{t}{T_V} - A_0)^2 \qquad (1.18)$$

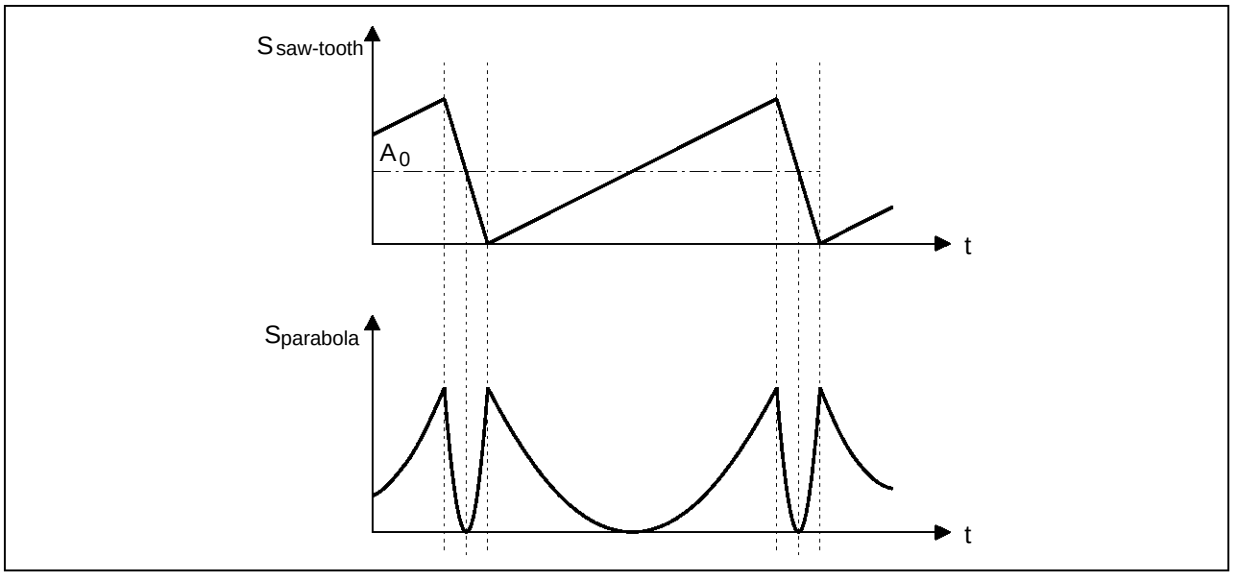
and is illustrated in Figure 12.

Thereby, k is the gain and A_0 is a DC-level which allows to adjust the symmetry of the parabola ("trapezoidal" or "keystone" correction).

Comparing the two methods, the following properties are evident :

- the parabola amplitude using the integration method is frequency dependent : assuming a constant amplitude of the saw-tooth signal, the amplitude of the parabola is linear in the time period T_V (see 1.16) . This means different adjustments between 50 and 60Hz TV-sets. The functional (square) method gives a frequency-independent amplitude of the parabola, if a constant saw-tooth signal is provided.
- during the flyback time of the saw-tooth signal, the functional network produces a second (parasitic) parabola as shown in Figure 12

Figure 12 : Generation of the Parabola with Functional Network



Although this parasitic parabola is present during the vertical flyback time (dark screen) this small parabola (like a spike) produces a damped oscillation of the diode modulator. The result is a damped sinusoidal vertical line on the top of the screen, if a test-grid is on the screen (the vertical lines are similar to a crutch-stick).

The maximum amplitude of this oscillation is present on the left and right top of the screen. Though its amplitude is normally only about 3mm, this effect must be suppressed.

This can be reached by two different methods :

- the linear saw-tooth voltage generating the parabola must have an extremely small flyback time. Then the very small parasitic parabola is integrated in the capacitor C_K of the comparator and has no effect (see Figure 7). The saw-tooth voltage coming from the vertical oscillator fulfills this requirement wherefore the deflection yoke-current has a too large flyback time.
- another possibility is to hold the parabola signal constant during the flyback time as illustrated in Figure 13.
  This behaviour can be reached by providing a parabola output limitation and then overmodulating the functional network during the flyback time.

Overcoming the problems of the parasitic parabola, the functional method should be preferred due to the independence of the frequency (50/60Hz compatibility).

The nonlinearity which forms the parabola can be realized in two different ways :

- use of an analog multiplier
- forming a nonlinear network by piece wise linearization.

I.5 - ADJUSTMENTS

I.5.1 - Horizontal size adjustment

Adjustment of horizontal amplitude is made by modifying the mean cyclic ratio (duty factor) of the output pulses. When this mean cyclic ratio is minimum, the picture width is maximum, because the output is more frequently in the low state, and therefore the highest current is drawn from the diode modulator and the deflection current is maximum.

To change the mean cyclic ratio of the pulse train (in addition to the change due to the parabolic shape of the signal) it is necessary to change the continuous level of the sawtooth pulse train (see Figure 14).

The rise of the continous level of the parabola is due to the increase of the cyclic ratio, as we have seen above. The value of pincushion correction is not modified since the parabola peak-to-peak amplitude is kept the same. Only the mean cyclic ratio varies, i.e. also the horizontal scan width.

I.5.2 - Pincushion correction adjustment

Pincushion correction is made by varying the peak-to-peak amplitude of the parabola. The greater this amplitude,the greater the variation of the output signal cyclic ratio is between the ends and the top of the parabola, and therefore the more important is the parabolic modulation of the current drawn from the diode modulator (see Figure 15).

Figure 13 : Modified parabola : constant during the flyback time

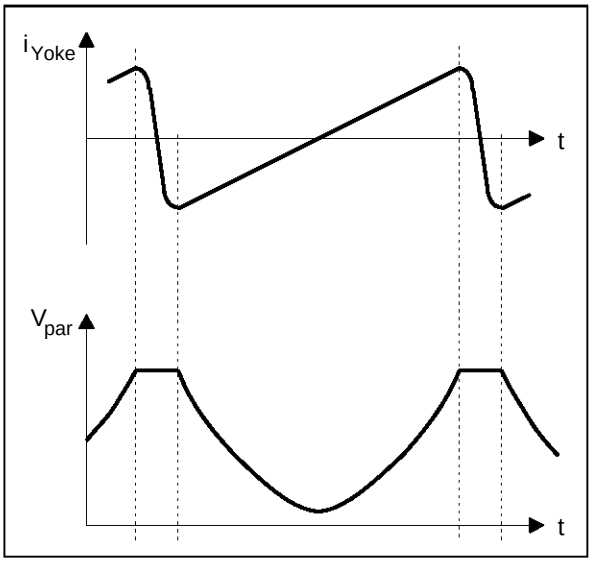


Figure 14 : Horizontal Size Adjustment

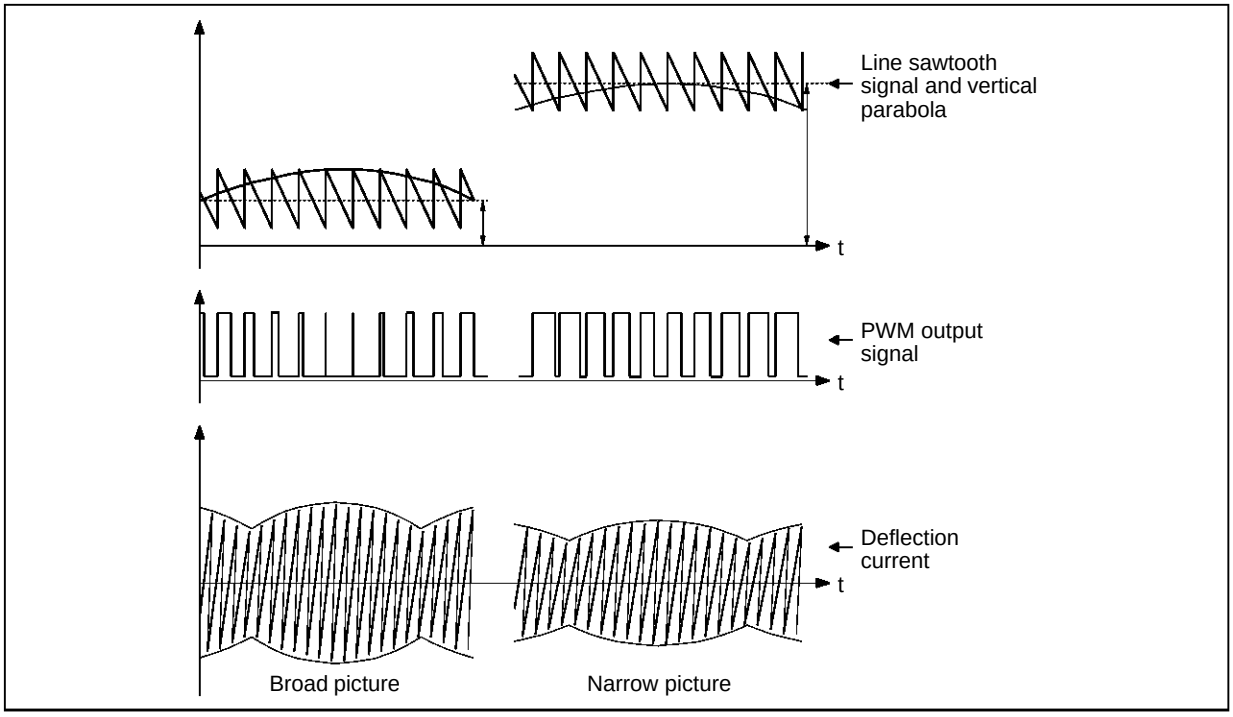
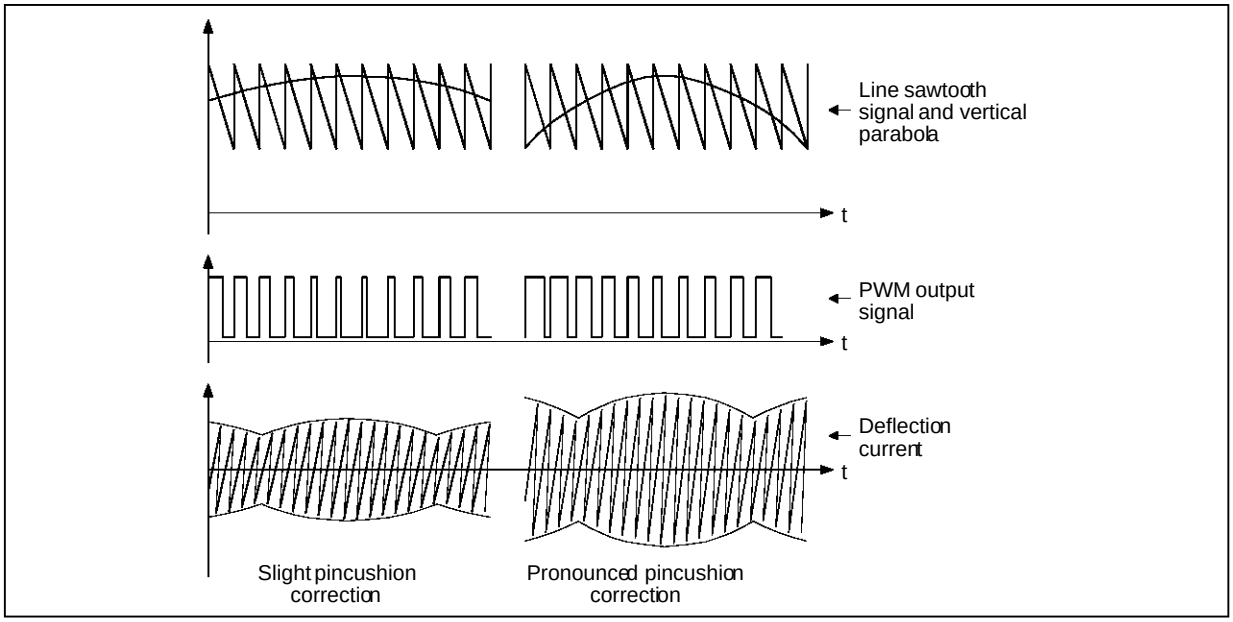


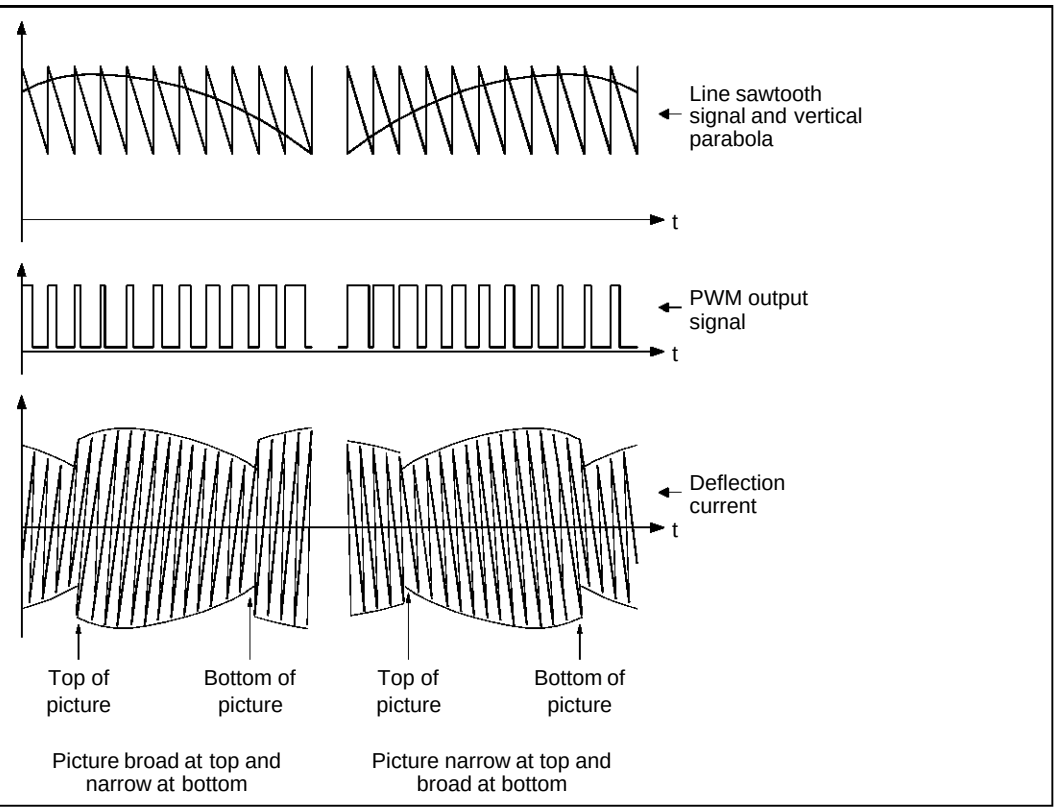
Figure 15 : Pincushion Correction Adjustment



I.5.3 - Trapezium correction adjustment (keystone correction)

Trapezium correction is made by modifying the symmetry of the left and right sides of the parabola (Figure 16).

Figure 16 : Keystone Correction



I.6 - PRODUCTS PRESENTATION

All the East/West correction devices are with class D diode modulator driver. Concerning the frame parabola generation, TDA4950, TDA8145 and TDA8146 use a non-linear network whereas TEA2031A uses an analog multiplier. TDA4950 and TDA8145 generate a parabola with a fixed shape; this shape is different between the two devices and makes the TDA4950 intended for standard CRT and TDA8145 for square tubes. These two devices have a parasitic parabola suppression (during vertical flyback time) by current limitation. TDA8146 has a programmable parabola shape generation by segments which makes it suitable for different CRTs. It has also a parasitic parabola suppression by pulse during vertical flyback.

All the devices can support a keystone correction adjustment (parabola symmetry) and have 50/60Hz capability. Some others adjustments are possible (picture width...).

Finally, another available device the TDA8147 has been designed for use in the East/West pincushion correction by driving a diode modulator but since this device has not the parabola generator and is drived by a PWM, it is very useful in digital TV-sets.

A detailed description about all the devices is done in the next chapters.

II - TEA2031A GENERAL DESCRIPTION

II.1 - INTRODUCTION

The TEA2031A circuit comprises (see Figure 17) : an analog multiplier that uses a frame sawtooth signal applied on Pin 1 so that the current on Pin 7 has a parabolic modulation.
This multiplier operates in current differential mode and uses a reference DC voltage, selected according to the continuous level of the sawtooth voltage, and applied on Pin 2.
The level of this DC voltage also serves to correct trapezium distortion.

- a reference voltage available on Pin 3 that can be used (via a voltage divider) to provide input 2 of the multiplier with a reference voltage.
- a current generator, producing a line frequency sawtooth signal by integrating the line flyback signal and generating current available on Pin 8.
- a comparator controlling the output stage by using the line sawtooth signal applied on its +input (Pin 8) and the parabolic signal generated by the multiplier and applied on its -input (Pin 7).

An output stage that can absorb or deliver current and comprises a diode connected to the DC voltage supply in order to limit the voltage applied on the output terminal during line flyback. This stage enables the diode modulator of the line scan circuit to be driven directly with a maximum current of 0.5A.
This maximum current that the output can absorb is not limited by the size of the transistors but by the maximum power dissipated by the package (Minidip).

II.2 - PARABOLA GENERATION

Using a fixed continuous current and a vertical sawtooth current, the multiplier generates an output current on Pin 7 with parabolic modulation.

II.2.1 - Multiplier stage operation

The multiplier inputs (Pins 1 and 2) operate in current differential mode (Figure 18).

Figure 17 : Block Diagram

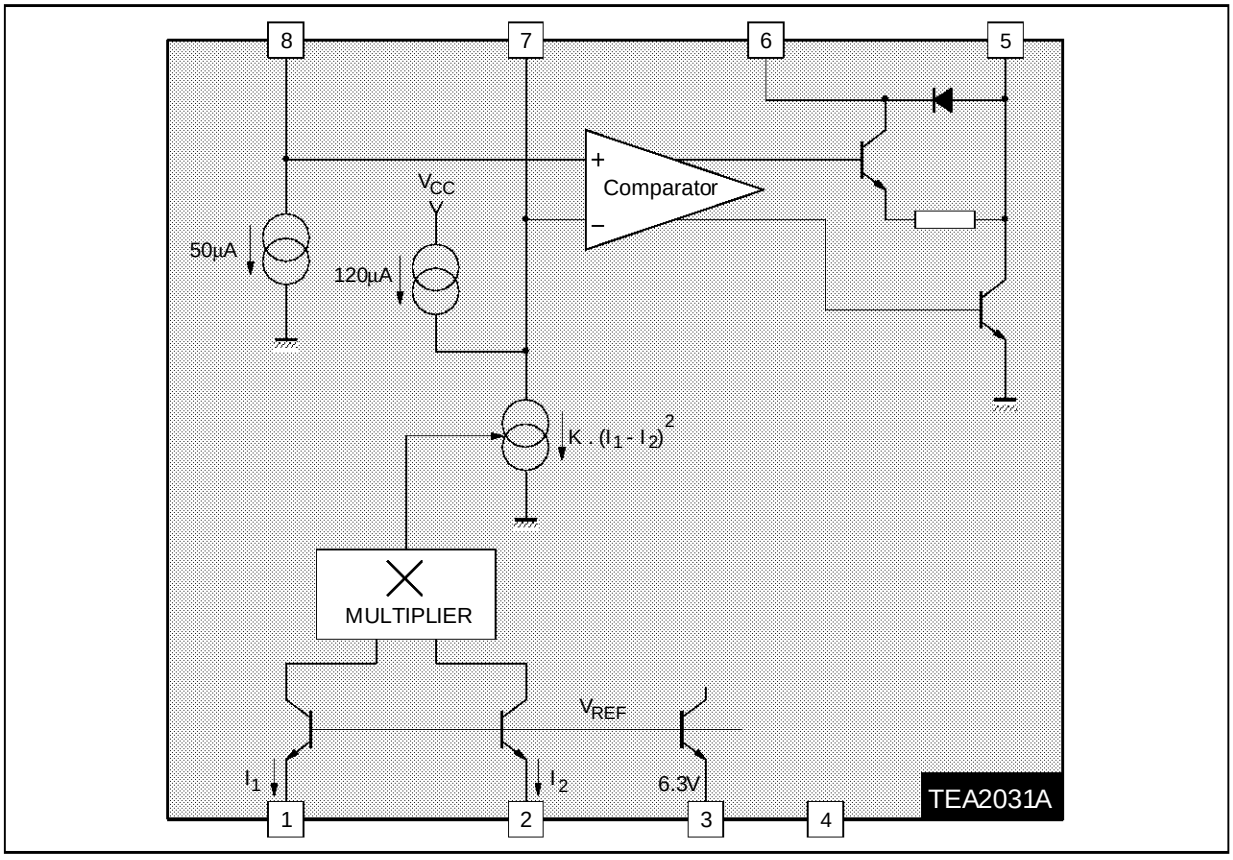
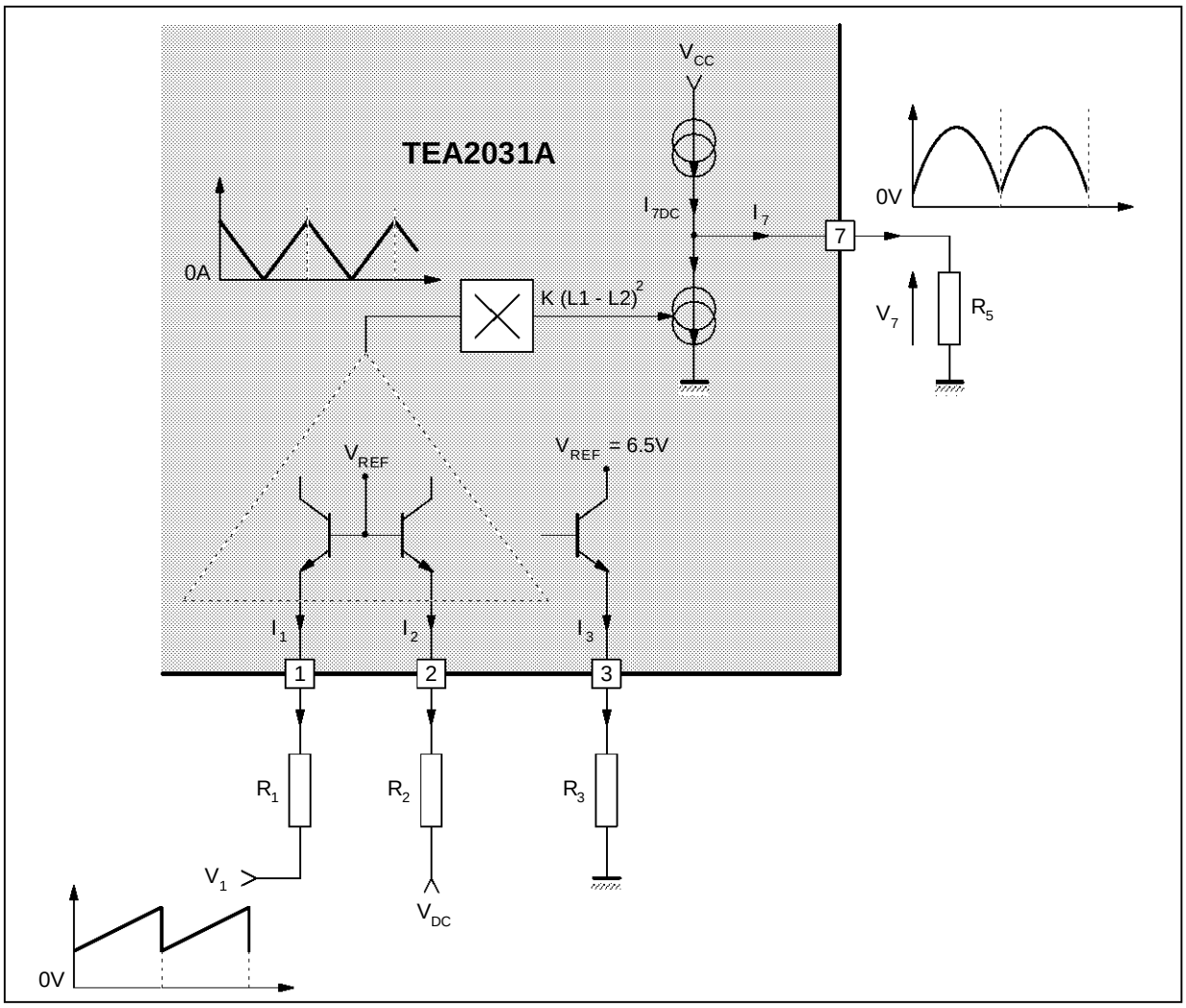


Figure 18 : Multiplier Stage



The output current is given by :

$$i_7 = i_{7DC} - k\,(i_1 - i_2)^2$$

i_{7DC} and k depend on the current reference on Pin 3.

Remarks : As we can see, the two inputs can be inverted and the slope of the sawtooth has no influence on the parabola shape.

II.2.1.a - Operation without keystone correction

In order to eliminate supply and thermal drift influences, R_1 is taken equal to R_2. In this case, $V_{1DC} = V_{2DC}$ (Figure 19).

II.2.1.b - Operation with keystone correction

In order to correct keystone correction, V_2 voltage becomes adjustable. In this case, the parabola shape presents a dissymmetry (Figure 20).

II.2.1.c - Example of applications

1. Sawtooth coming from the horizontal:vertical processor (e.g. TDA8185, TEA2028B, ...)
   In this case, V_{1DC} = 2.5V (Figure 21).
   For practical reason, the DC voltage comes from internal voltage reference. Impedance value seen between Pin 3 and ground must be 22kΩ for best conditions of operation (to have the good internal current reference).
2. Sawtooth coming from the vertical output stage (Figure 22)
   In this case V_{1DC} = 0V and $R1 = R2 + \frac{1}{2} RT2$

Figure 19 : Operation without Keystone Correction

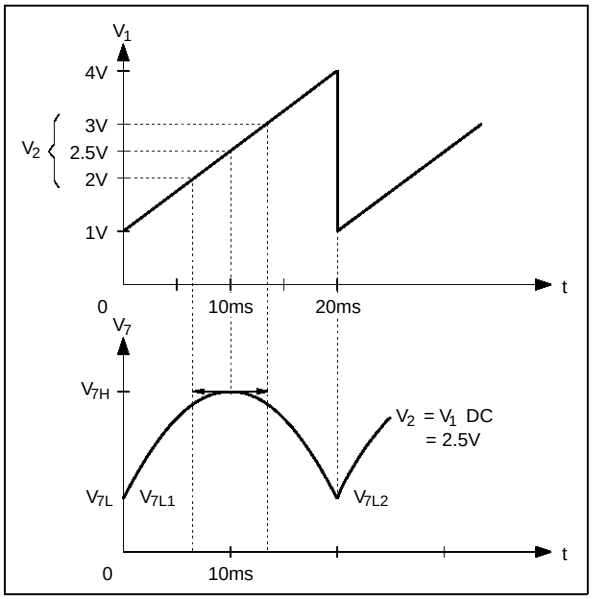


Figure 20 : Operation with Keystone Correction

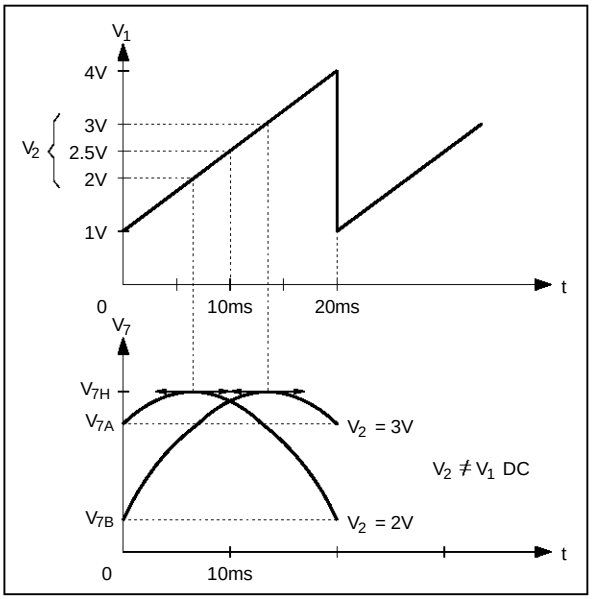


Figure 21 : Sawtooth coming from H/V Processor

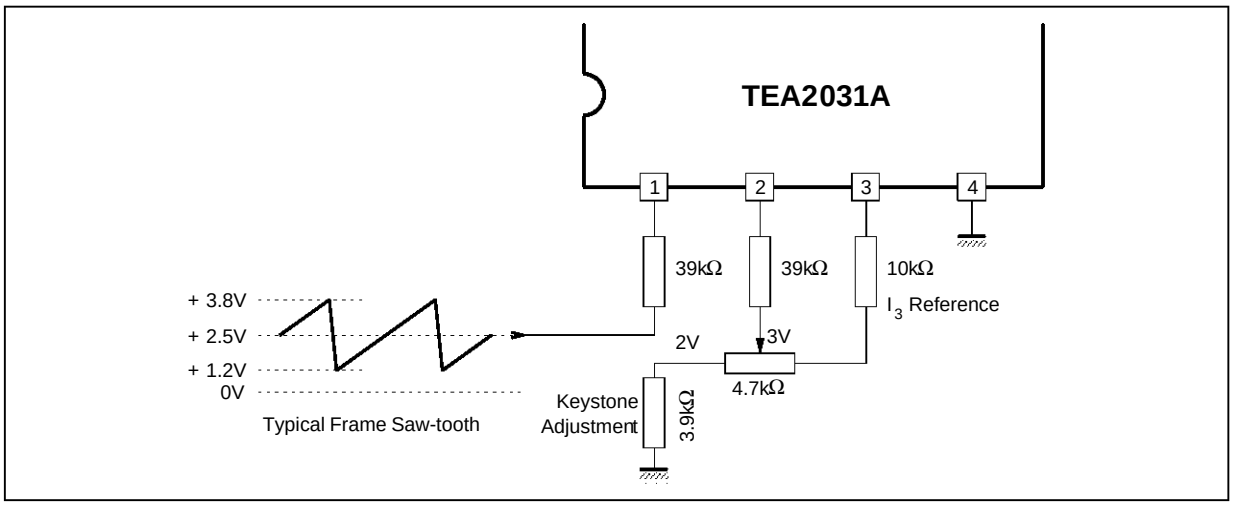
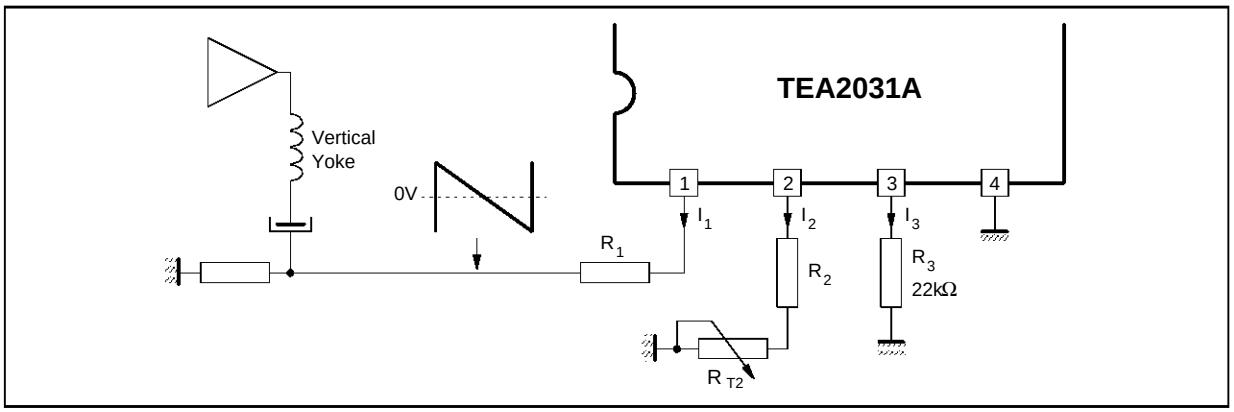


Figure 22 : Sawtooth coming from Vertical Output Stage



II.3 - LINE SAWTOOTH GENERATION

The line sawtooth signal is applied as a reference at the +input terminal of the comparator. It is obtained by integrating the line flyback and the constant current discharge of capacitor C3 in Pin 8 (Figure 23).

II.3.1 - Role of resistors R7, R8, RT1 and D2

By means of the voltage divider bridge comprising resistors R7, RT1 and R8, a signal that is the image of the line flyback signal applied on R7, is obtained on the slide contact of potentiometer RT1. The peak amplitude of this signal depends on the nominal voltage of the Zener diode D2 and on the adjustment of RT1.

The role of Zener diode D2 is to maintain a constant amplitude of the signal on the slide contact of RT1 whatever the variations in amplitude of the line flyback signal.

This diode D2 can be also replaced by a single diode connected to a regulated 12V or 15V power supply.

II.3.2 - Role of diode D1 and capacitor C3

During line flyback, diode D1 rapidly charges capacitor C3 at the potential available on the slide contact of RT1.

Then during line scanning, D1 is blocked and C3 is discharged at constant current (about 50µA) through Pin 8.

The peak-to-peak amplitude of the line frequency sawtooth signal obtained in this way depends directly on the value of capacitor C3 since it is defined by the discharge current of the capacitor and the line period (Figure 24).

This amplitude can be calculated using the following equation :

$$V_{8\ (peak\text{-}to\text{-}peak)} = \frac{dt \cdot i_8}{C3}$$

where Dt = duration of line and i_8 = current in Pin 8.

The continuous level of this sawtooth signal is set by adjusting potentiometer RT1 (Figure 25).

Figure 23 : Line Sawtooth Generation

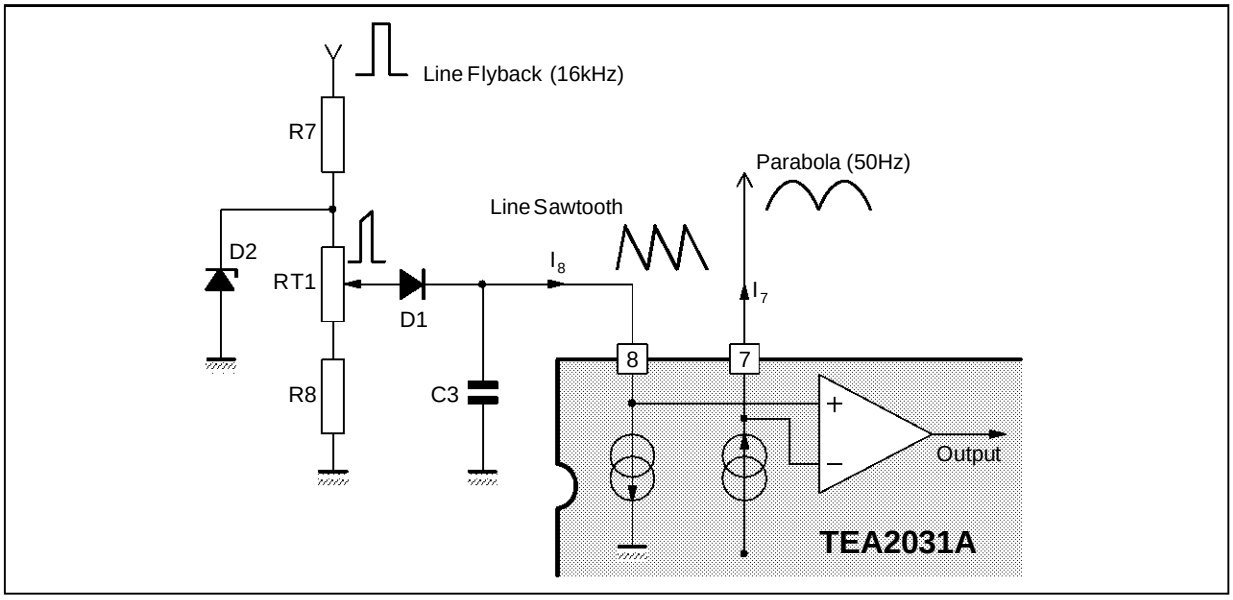


Figure 24 : Peak-to-peak Amplitude of Sawtooth Signal versus Two Different Values of C3 (with RT1 = constant)

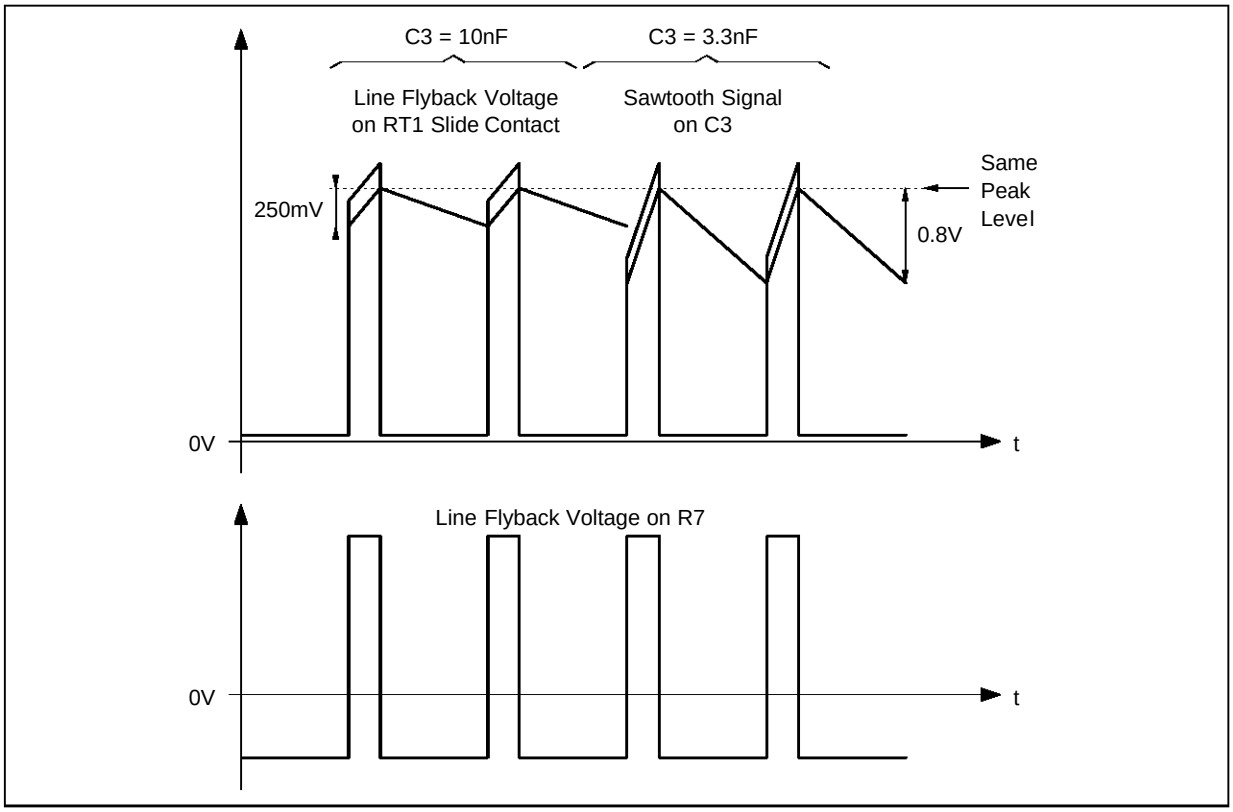
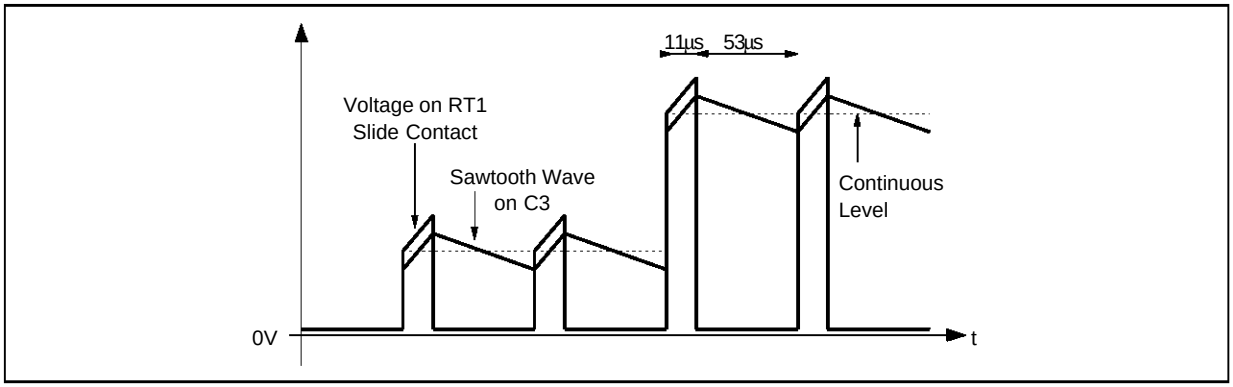


Figure 25 : Continuous Level of Swatooth Signal for Two Different Adjustments of RT1



II.4 - OUTPUT STAGE

The output stage is controlled by the comparator fed by signals applied on its inputs, i.e. the sawtooth signal at line frequency on +input (Pin 8) and the parabola at vertical frequency on -input (Pin 7) (see Figure 26).
The comparison between the 50Hz parabola and the sawtooth signal at line frequency (16kHz) produces pulses at line frequency with a duty cycle that is modulated at vertical frequency. This allows, by means of the diode modulator, the modulation of the line scanning current during each field period in order to carry out the pincushion correction (or East/West correction) (see Figure 27).

The role of the filter C2 and RT3 + R6 is to suppress the line frequency of the feedback output signal.

Figure 26 : Output Stage

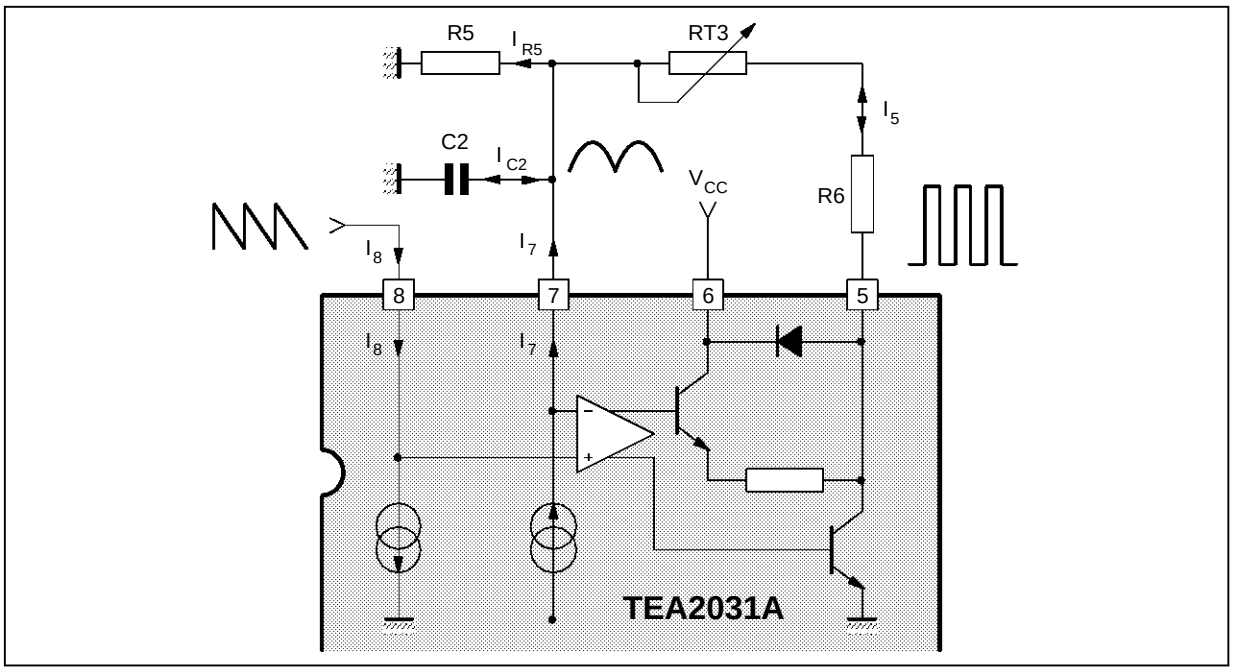
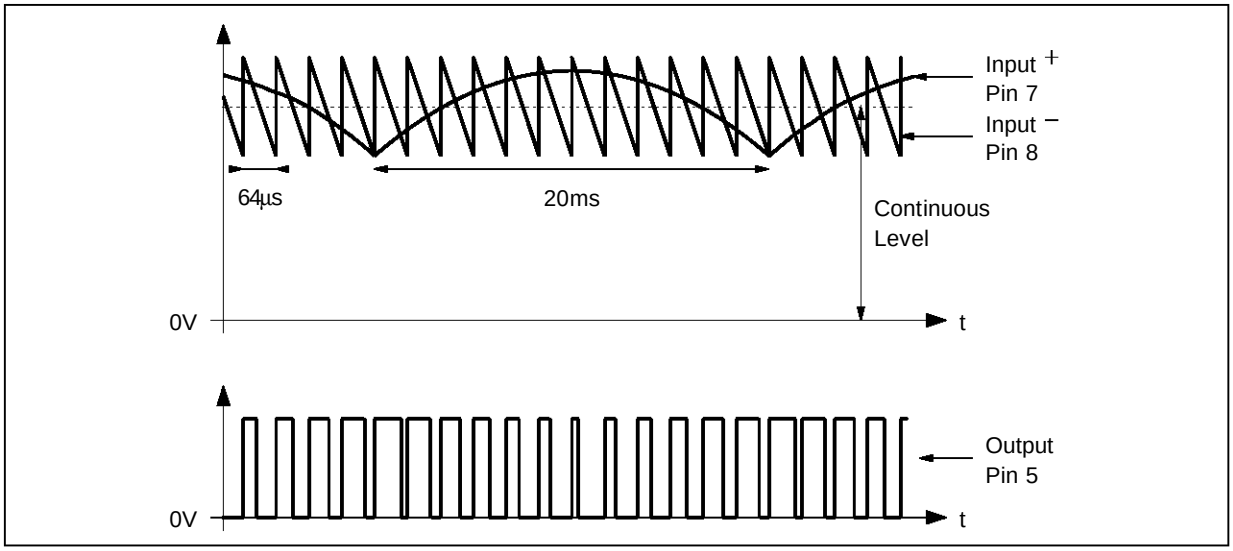


Figure 27 : PWM Output Signal (with adaptation of time scales)



II.4.1 - Operation of the Output Stage

The operation of the output stage can be considered as 3 separate cases according to the 3 possible states of output Pin 5.

II.4.1.a - Output in the low state (Figure 28)

In this case resistances R6 and RT3 are connected to the ground, therefore they are in parallel with R5, according to the following diagram.

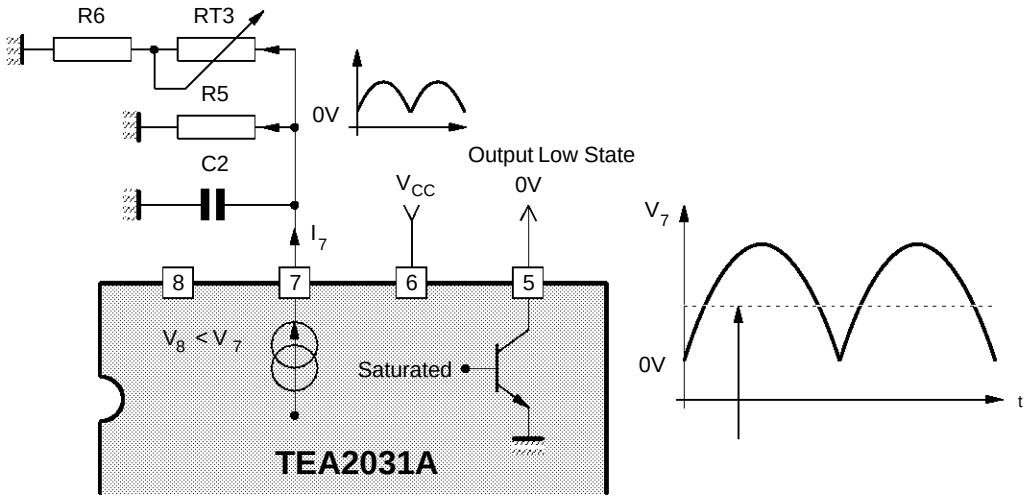
The continuous level and the peak-to-peak amplitude of the parabola are at their minimum when the RT3 value is minimum.

It is possible to calculate the voltage for a given point of the parabola (Pin 7) using the following equation :

$$V_{7b} = i_7 \cdot \frac{R5 \cdot (R6 + RT3)}{R5 + R6 + RT3}$$

The capacitance of C2 is neglected as this capacitor is equivalent to an open-circuit at vertical frequency.

Figure 28 : Output in Low State



II.4.1.b - Output in the high state

In this case, resistances R6, RT3 and R5 form a voltage divider bridge which returns on Pin 7 and capacitor C2 part of the continuous voltage available on the output terminal that is added to the parabola voltage.
The equivalent circuit diagram is the following : see Figure 29.

It is possible to calculate the voltage for a given point of the parabola (Pin 7) with the following equation :

$$V_{7h} = i_7 \cdot \frac{R5 \cdot (R6 + RT3)}{R5 + R6 + RT3} + V_5 \cdot \frac{R5}{R5 + R6 + RT3}$$

II.4.1.c - Output with commutation

In this case and if capacitor C2 is eliminated, Figure 30 gives the signal obtained on Pin 7. It corresponds exactly to the levels and amplitudes of the parabolas for output in the high state and the low state, linked by 16kHz commutations.
In normal circuit configuration, capacitor C2 is connected and constitutes a filter with R6 and RT3. The preceding signal is filtered and is transformed into the signal shown in Figure 31.
The 16kHz line frequency component has disappeared in the signal and only the 50Hz parabola remains, but slightly modulated at line frequency by the C2 charge when the output is in the high state, and by the C2 discharge when the output is in the low state; this gives a tiny triangular modulation signal.

So the continuous level of the parabola depends only on the cyclic ratio of the output pulse train. This level can be calculated by means of the following equation : $V_{mean} = M \cdot V_{7h} + (1 - M) \cdot V_{7b}$

where

M : output pulse cyclic ratio
V_{7h} : mean level on Pin 7, output blocked in the high state
V_{7l} : mean level on Pin 7, output blocked in the low state

Figure 29 : Output in High State

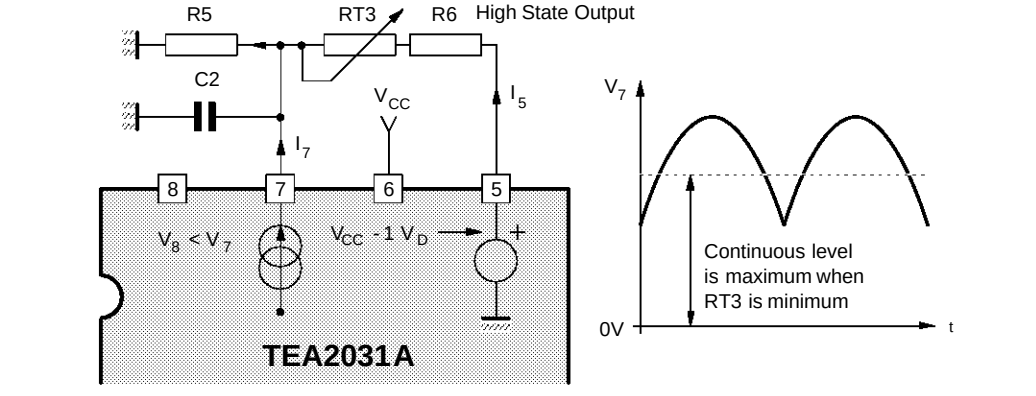


Figure 30 : Output with Commutation (without C2)

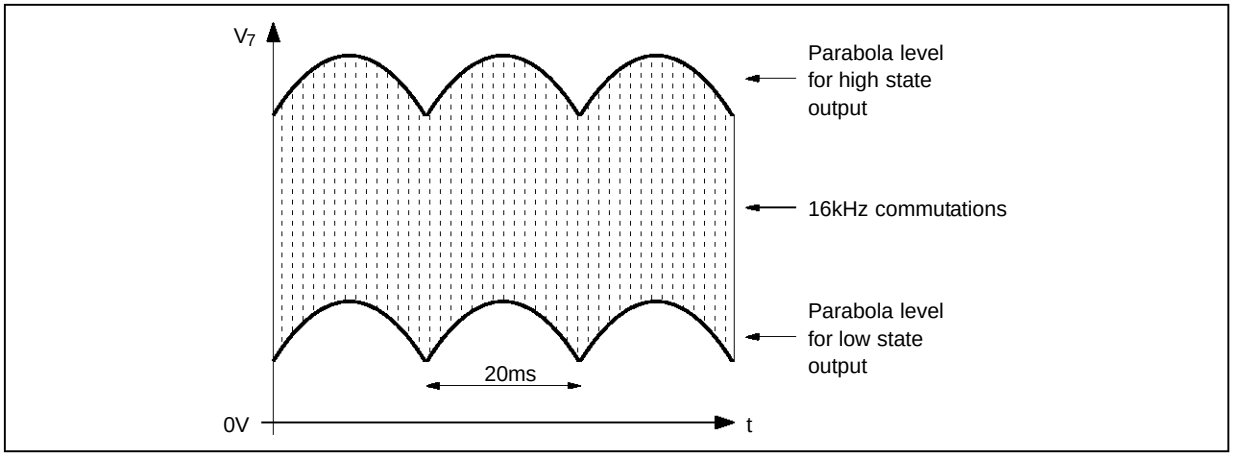
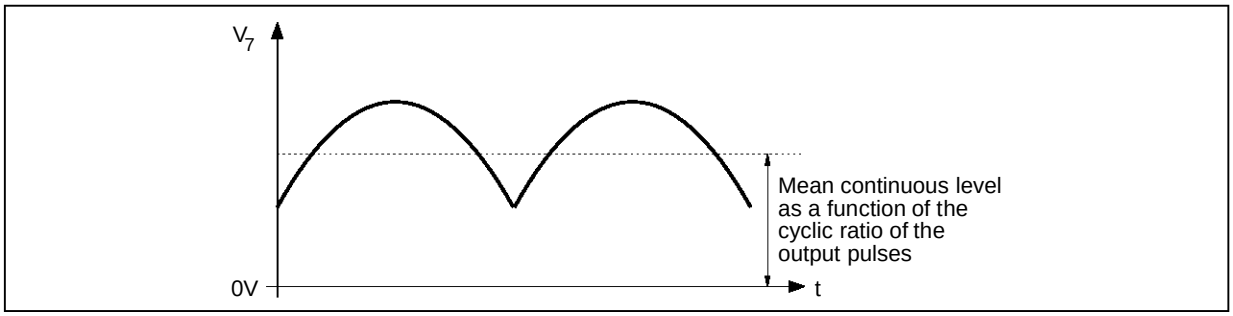


Figure 31 : Output with Commutation (with C2)



We see that, when the cyclic ratio increases, the continuous level of the parabola also increases and approaches its maximum level when the output is in the high state. Conversely, when the cyclic ratio decreases, the continuous level of the parabola also decreases since it approaches its minimum continuous level when the output is in the low state.

II.4.1.d - Conclusion

For a given parabolic current i_7, the parabola peak-to-peak amplitude depends only on resistance values R5,R6 and RT3. Therefore by adjusting RT3, it is possible to obtain a more or less pronounced parabola and so adjust the importance of pincushion correction.

The continuous level of the parabola depends principally on the mean cyclic ratio at the output, and much less on the adjustment of RT3.

II.4.2 - Operation in association with the diode modulator (see Figure 32)

In the majority of cases, the system operates by drawing more or less high current from the modulator through the connecting inductor. The current through terminal Pin 5 of TEA2031A is entering into the circuit. It flows, either to the ground when the output is in the low state, or to V_{CC} through the internal diode when the output is in the high state and the output voltage tends to exceed V_{CC}. The circuit can also produce current.

Figure 32 : Operation with Diode Modulator

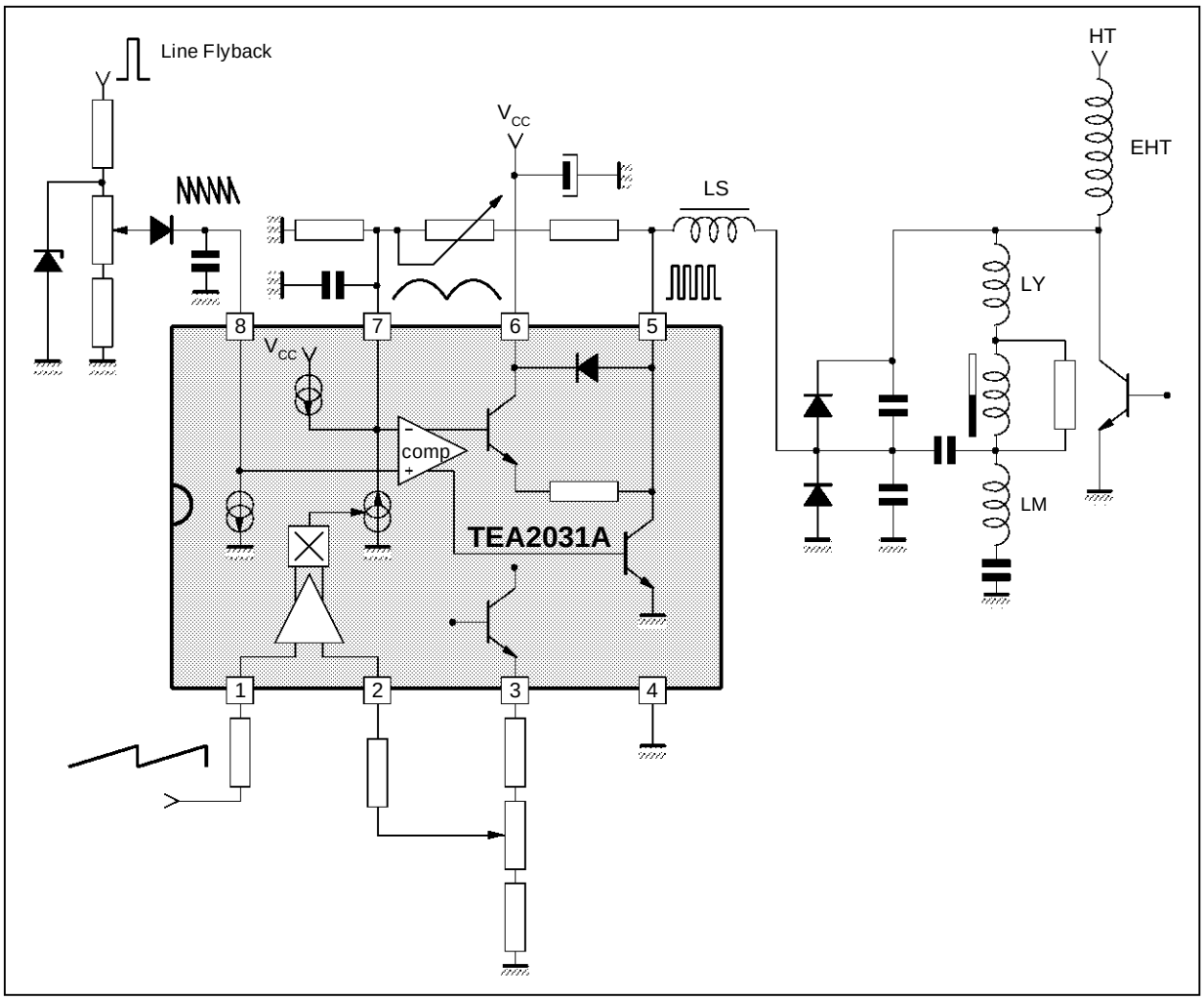
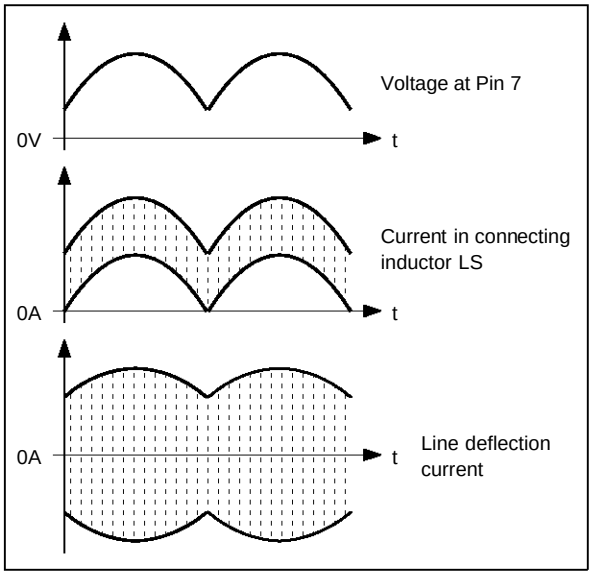


Figure 33 : Output Oscillagrams



II.5 - SELECTION OF THE VALUES OF CAPACITORS C2 AND C3

Correct operation of TEA2031A depends partly on the choice of these values for two reasons :

- for a given amplitude of the parabola, the importance of final pincushion correction at the output of TEA2031A is determined by defining, by means of C3, the amplitude of the line sawtooth wave.
- the absence of oscillation at circuit output is controlled through adjustment of the value of C2 as described below.

II.5.1 - Selection of C3

As seen before (chapter II.3.2), the value of C3 and only this value (in the limits of the available voltage on the slider of RT1) can fix the value for the amplitude of the line sawtooth wave. Now this amplitude must be greater than the parabola am-

plitude (Pin 7) but not so far in order to have a correction amplitude sufficient but permitting also an horizontal amplitude adjustment :

- if the line sawtooth wave and the parabola have the same amplitude, the pincushion correction is maximum but the horizontal amplitude adjustment range is non-exutent
- if the line sawtooth amplitude is much greater than the parabola's one, we will have a large range for the horizontal amplitude adjustment, but it will be to the detriment of the pincushion correction amplitude.

Once the desired line sawtooth amplitude has been fixed, we can calculate the value of C3 with the following formula

$$C3 = \frac{Dt \cdot i_8}{V_8}$$

where

Dt : line scan duration (around 53µs)
i_8 : Pin 8 current (around 50µA)
V_8 : line sawtooth peak-to-peak amplitude (Pin 8)

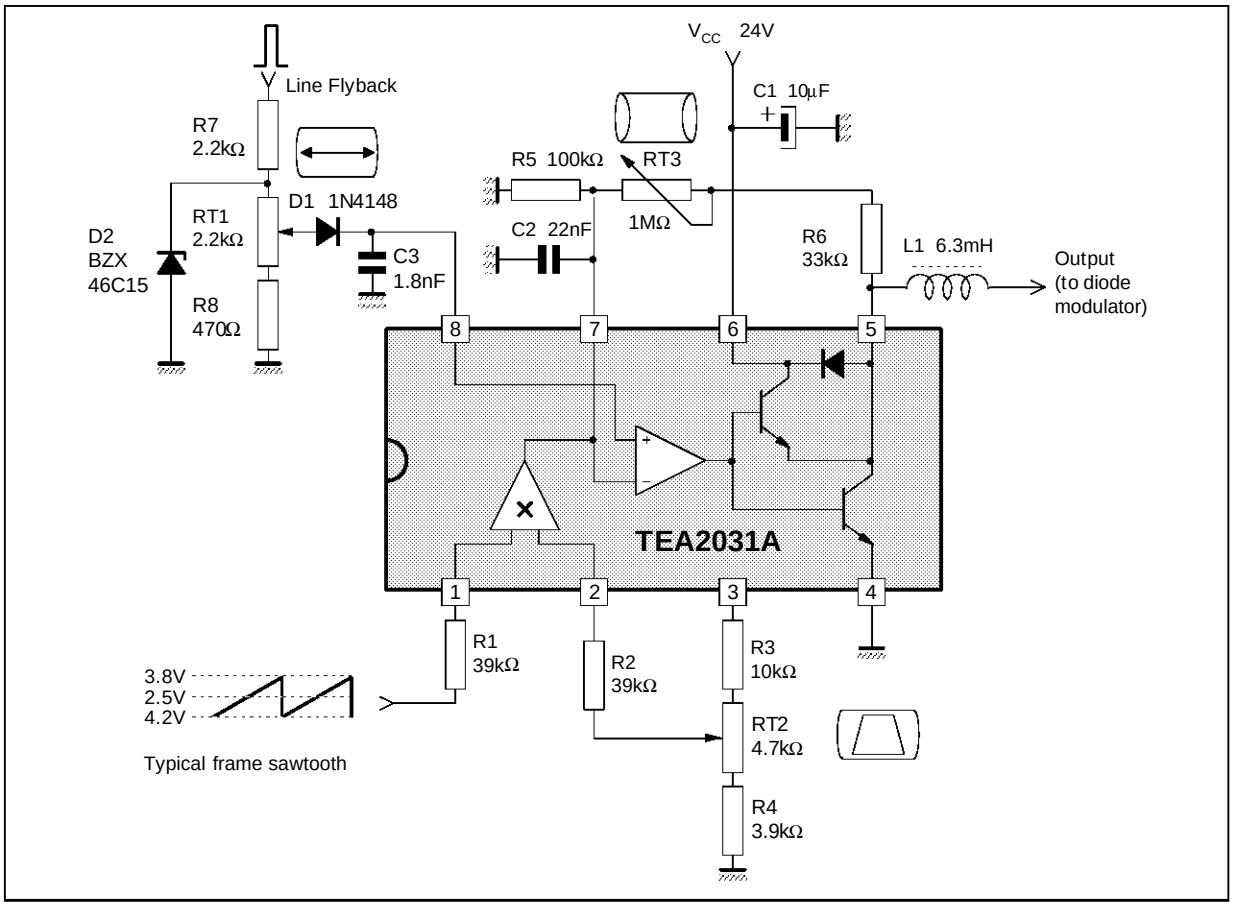
II.5.2 - Selection of C2

The selection of C2 is related to the values of R5, R6 and RT3. The value of C2 must be large enough to avoid any risk of oscillations at output for the entire range of adjustment of potentiometers RT1 and RT3. The value of C2 must be small enough not to influence the shape of the vertical frequency parabola.

II.6 - APPLICATION EXAMPLE

A typical application diagram is given in Figure 34.

Figure 34 : Typical Application



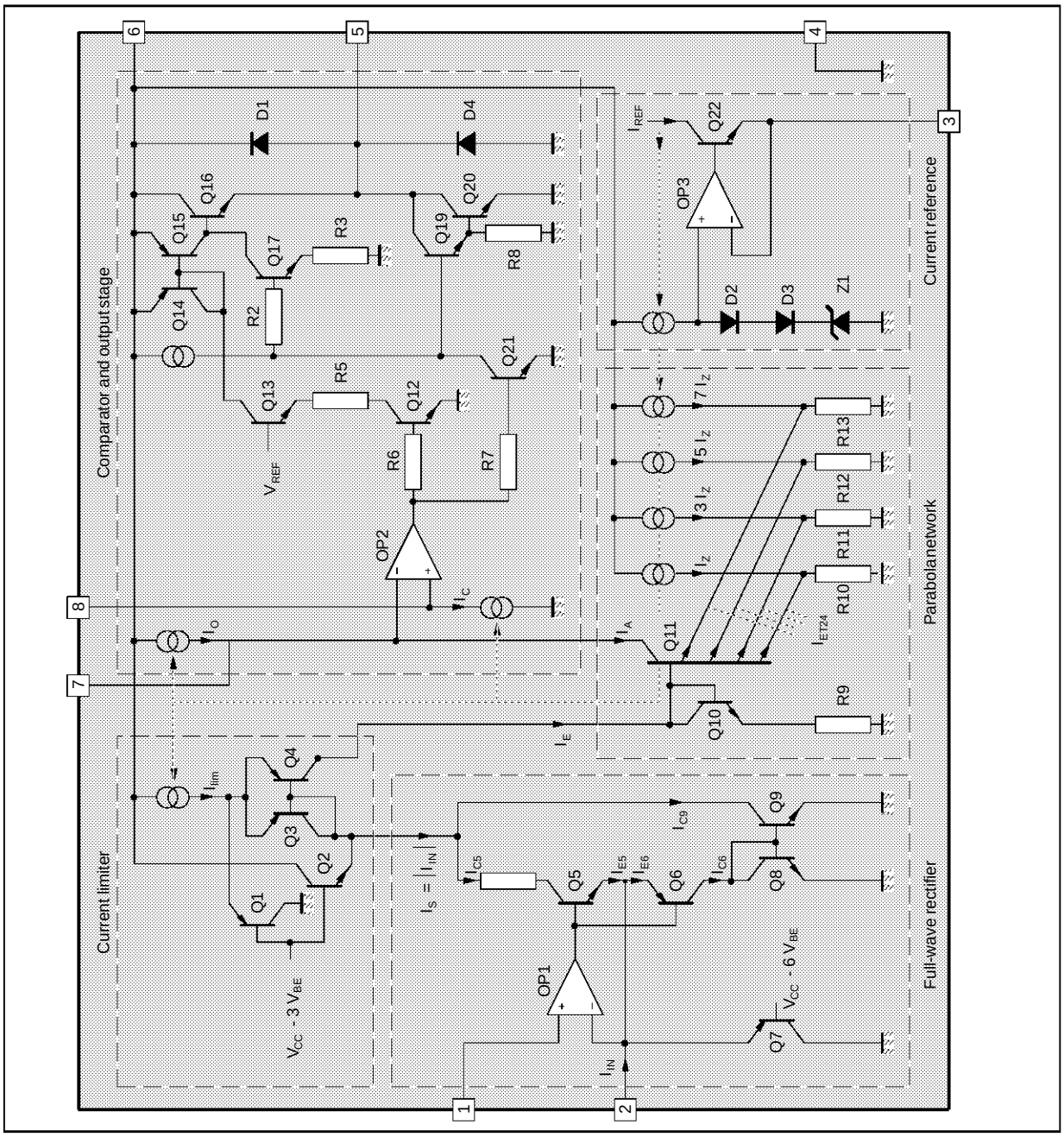
III - TDA4950 - TDA8145 GENERAL DESCRIPTION

III.1 - INTRODUCTION

The TDA4950 and TDA8145 consist mainly of 5 parts as seen in the simplified circuit diagram (Figure 35).

1. Full-wave rectifier for the input current I_{IN}.
2. Current limiter in order to limit the rectified current I_{IN} to the maximum value of 40µA (with this functional block a suppression of the parasitic parabola is possible, see chapter I.4).
3. Parabola network producing the current $I_A = k(I_{IN})^2$ (k = constant).
4. Comparator and output stage working as a pulse-width modulator for driving the diode modulator.
5. Voltage reference and current reference which produces the reference current I_{REF} via external resistor RI between Pin 3 and Ground.

Figure 35 : Simplified Circuit Diagram for TDA4950 - TDA8145



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III.2 - DESCRIPTION

Let us consider the blocks in detail :
The input amplifier OP1 drives the transistor Q5 or Q6. They offer two different signal paths, depending on the sign of the input current I_{IN}.
Assuming that I_{IN} is negative, the feedback loop is closed via the transistor Q5 and the output current I_{C5} is given by

$$I_{C5} = I_{E5}\left(\frac{\beta_5}{1+\beta_5}\right) = -I_{IN}\left(\frac{\beta_5}{1+\beta_5}\right)$$

where β_5 is the current gain of the transistor Q5. β_5 can be assumed to be more than 100, so the mismatching between I_{C5} and I_{IN} is less than 1%.
For a positive current I_{IN} the output voltage of OP1 decreases : Q5 is switched off the current I_{IN} is the emitter current I_{E13} of Q6.
Its collector current I_{C6} is given by

$$I_{C6} = I_{IN}\left(\frac{\beta_6}{1+\beta_6}\right)$$

Since the maximum input current is 40µA, the current gain of this PNP transistor is still high enough to give a reasonable small error. This current biases the current mirror Q8 and Q9. A good matching between the current I_{C8} and I_{C9} must be provided. Thus the current I_S is given by

$$I_S = \begin{cases} -I_{IN}\left(\frac{\beta_5}{1+\beta_5}\right) & I_{IN} < 0 \\ +I_{IN}\left(\frac{\beta_6}{1+\beta_6}\right) & I_{IN} > 0 \end{cases}$$

Neglecting the base current of Q6 and Q5, I_S is nearly the absolute value of I_{IN}.
Note that for both signal paths, the OP1 has a feedback factor of 1. This means OP1 must be frequency compensated for unity gain.
The transistors Q3 and Q4 work as a normal current mirror if the current I_S plus I_E is smaller than the current I_{lim} :

$$2\ I_S < I_{lim}$$

In this case the excess current is shunted via the PNP transistor Q1.
If the current I_S becomes higher

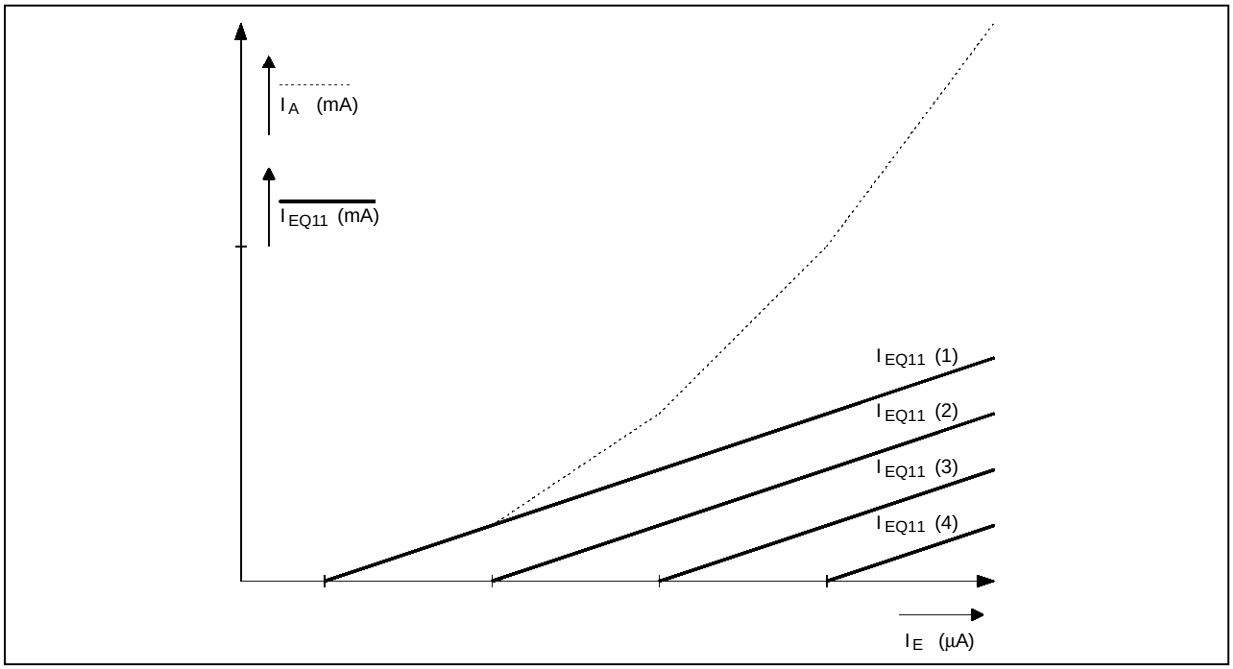
$$I_S > I_{lim}/2$$

the transistor Q1 switches off and Q2 picks up the current I_S from the rectifier which exceeds the maximum value of $I_{lim}/2$.
Using the proposed reference resistor RI between Pin 3 and Ground (11kΩ) the current I_E can be described with

$$I_E = \begin{cases} I_{IN} & I_{IN} < 40\mu A \\ 40\mu A & I_{IN} > 40\mu A \end{cases}$$

The parabola network produces an output current I_A which is approximately a parabola : $I_A = k\ I_E^2$
The parabolic behaviour I_A is obtained via piecewise linear approximation. For this purpose the identical resistors R_Z are connected with the four emitters. The four different biasing currents i_Z, $3i_Z$, $5i_Z$, $7i_Z$ yield four different threshold voltages, so the four emitter currents of Q11 are switched stepwise. A schematic illustration of the single emitter currents I_{EQ11} (1...4) of Q11 as a function of the current I_E is given in Figure 36.

Figure 36 : Transfer Characteristic of the Parabola Network

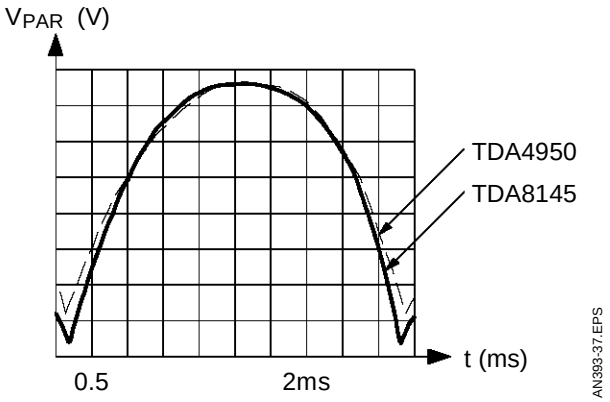


Due to the exponential character of the emitter current as a function of the base emitter voltage, the output current I_A is smoothed.
For designing the values of R_Z and i_Z of this parabola network we must take a compromise between the smoothing effect and the temperature dependence. Small values of R_Z and i_Z yield small threshold voltages for the 4 emitters of Q11. This means a good smoothing of the edges, but a worse temperature dependence.

Large values of R_Z and i_Z yield the opposite result. Practical experiences show that a value of 0.5V for the 4th emitter (R13 $7i_Z$) for I_{IN}= 0 gives an acceptable cmpromise.

Due to different values of resistor R_Z, the TDA8145 is adapted to flat square tubes (see Figure 37 for the two different shapes of the parabola).

Figure 37 : Parabola Shapes for TDA4950 and TDA8145



The parabolic output current I_A produces a corresponding voltage drop across an external resistor between Pin 7 and Ground (18kΩ). The additional constant current source I_0 shifts the D.C. voltage level to achieve an appropriate operating point of the comparator. Its non-inverting input is connected with a horizontal saw-tooth voltage. For this purpose an external capacitor is connected with Pin 8 and Ground which is discharged with the internal current source I_C. It will be charged with the positive flyback pulses produced in the line transformer during the flyback time.

Due to the linear saw-tooth voltage on Pin 8 this comparator works as a pulse-width modulator.
The output of this comparator controls the output stage. If the output of the comparator OP2 is high, Q21 and Q12 are saturated. Therefore, the Darlington output transistor Q19, Q20 is switched off.

The transistor Q13 and the resistor R5 acts as a current source biasing the current mirror Q14, Q15. The transistor Q16 is switched on.

If the output of OP2 becomes low, Q12 and Q21 are switched off. In this case the current in Q14 and Q15 dissappears and Q16 is switched off. Synchronously the darlington stage Q19 and Q20 is saturated.

In order to achieve a fast commutation from Q16 to Q19/Q20 an active discharging of Q16 is provided with the aid of the transistor Q17.

During a normal operation range if the output current i_{OUT} is positive, only the Darlington stage (Q19, Q20) and the diode D1 are necessary to drive the external inductor. With the aid of Q16 and the intrinsic substrate diode D4 the output current i_{OUT} can become negative, too; so that the modulation range of the diode modulator becomes larger.

The Zener diode Z1 serves as the voltage reference. With the aid of the diodes D2 and D3, a good temperature compensation can be achieved.

Using an external resistor of R_I = 11kΩ between Pin 3 and Ground we get an accurate and temperature independent current reference to bias the internal current sources.

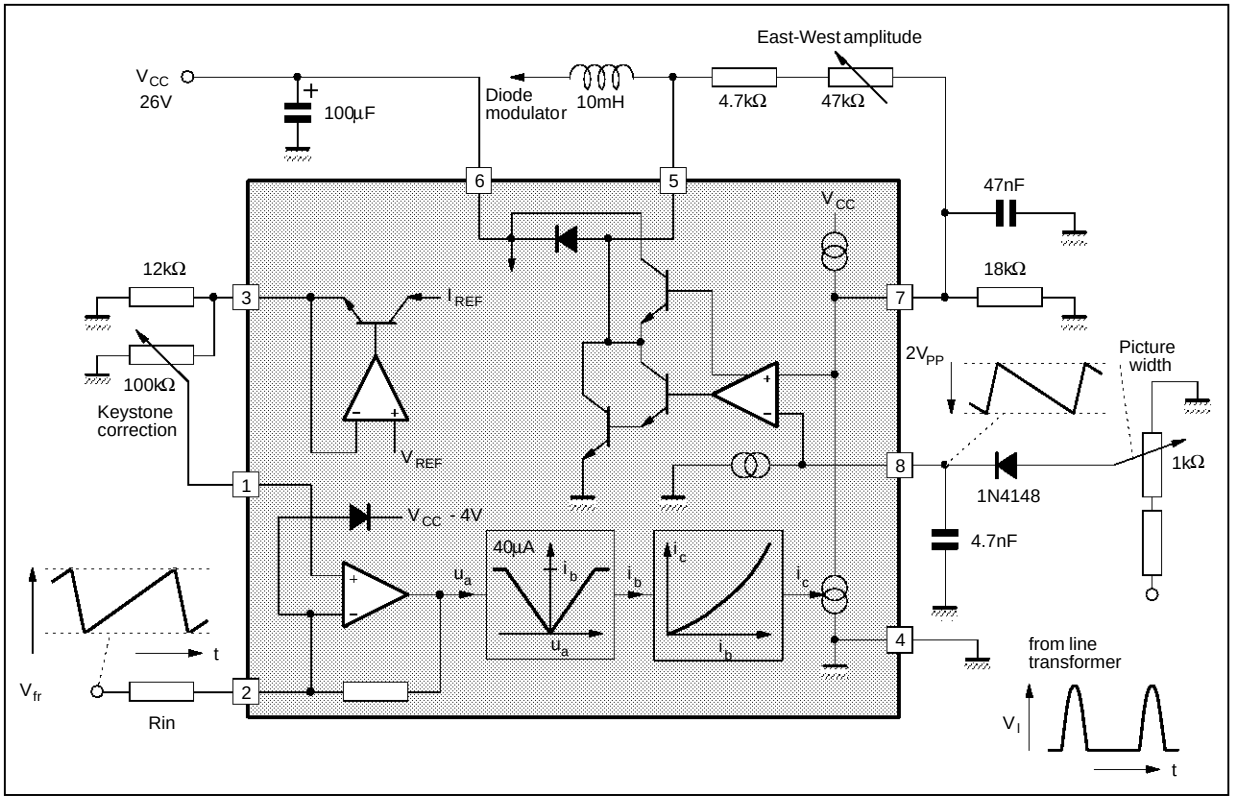
III.3 - APPLICATION

A standard application diagram is given in Figure 38.
Pin 2 is biased from a linear saw-tooth voltage, the resistor R_{IN} produces the input saw-tooth current. The non-inverting input (Pin 1) is connected with an adjustable voltage (keystone correction). With the aid of this trimmer, the symmetry of the parabola can be adjusted in order to correct a trapezoidal error in the colour picture tube. A further adjustment trimmer is responsible for the picture width and influences only the DC-level of the comparator input (Pin 8). (Since the discharging current sink on Pin 8 is constant, the amplitude of the horizontal saw-tooth voltage (V_{PP}) remains constant).

The thrid trimmer is in the feedback path and is responsible for the parabola correction factor. With the aid of this trimmer the distortion on the screen can be changed from pillow-distortion up to an over-correction (tun-distorsion).

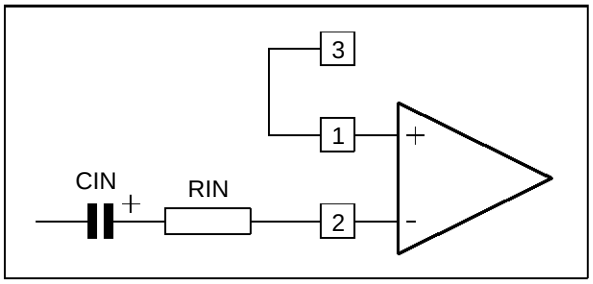
For some applications the keystone adjustment trimmer is not necessary (small trapezoidal error of the picture tube). In this case, a symmetric parabola should be produced.

Figure 38 : Standard Application Diagram of TDA4950 and TDA8145



This can easily be obtained by AC-coupling the input (Pin 2) as seen in Figure 39.

Figure 39 : AC-coupled Vertical Saw-tooth Voltage, no Keystone (trapezoidal) Correction



In order to avoid any distorsion, the time constant $C_{IN} \cdot R_{IN}$ should be at least 10 times larger than the time period ($C_{IN} \cdot R_{IN} > 10 \cdot 20ms$). On the other hand a too large time constant yields an undesired bouncing effect in the East/West correction.

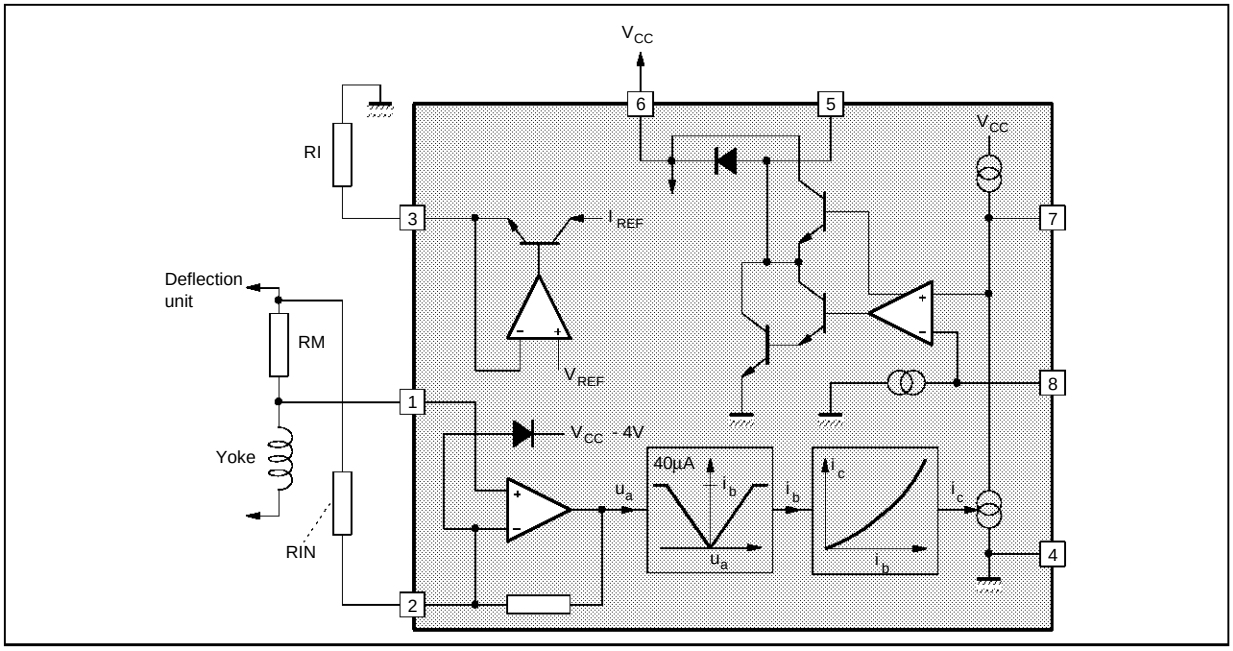
The DC voltage on Pin 1 is arbitrary.

For the sake of simplicity, connect Pin 1 with Pin 3.

Another possible application with parasitic parabola suppression is given in Figure 40.

The input current into Pin 2 is generated via the voltage drop on R_M. Due to the common mode rejection of the input operational amplifier, the voltage change during the vertical scan time (saw-tooth voltage) has nearly no effect. During the flyback time, a positive pulse (> V_{CC}) is present on Pin 1 and Pin 2. With this flyback pulse the current limitation in the parabola generation circuit is activated and limits the parabola amplitude. Since the flyback time is relatively long, this limitation is necessary to suppress the parasitic parabola (see chapter I.4).

Figure 40 : Application of TDA4950 and TDA8145 with Parasitic Parabola Suppression



IV - TDA8146 GENERAL DESCRIPTION

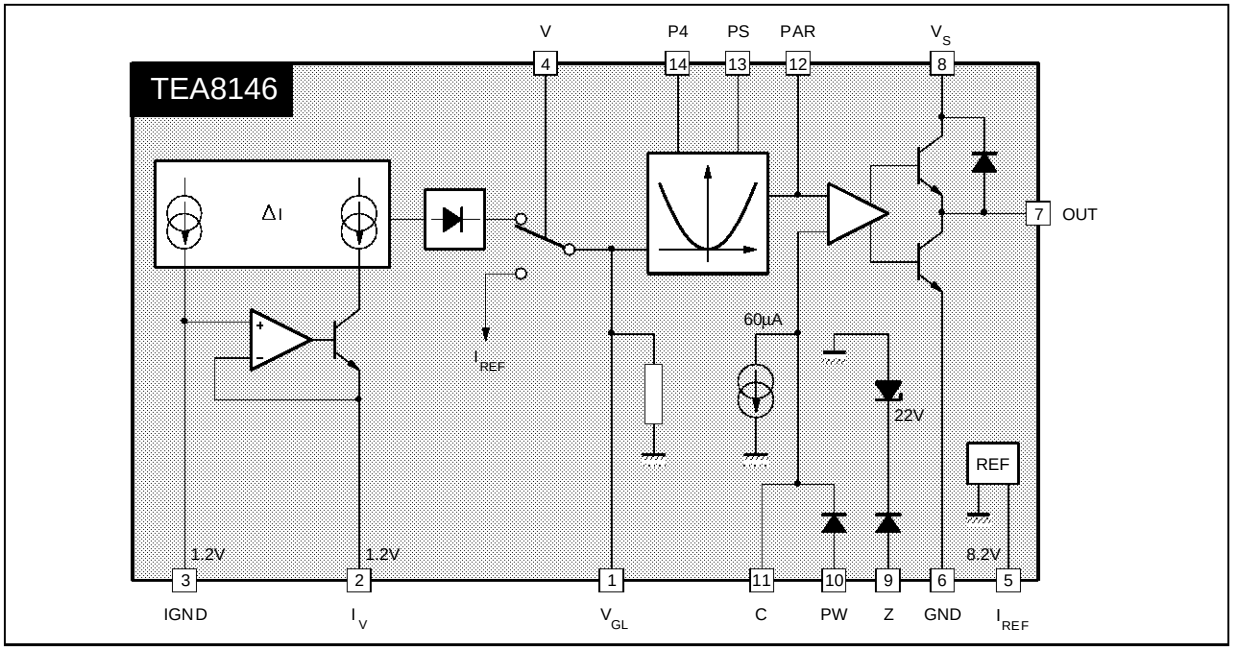
IV.1 - INTRODUCTION

The TDA8146 was designed for TV and monitor sets with various types of picture tubes, where a programmable parabola is mandatory. The complete block diagram is shown in Figure 41.

The following features confer to this IC an all-purpose suitability :

- programmable parabolic current generator
- parasitic parabola suppression during vertical flyback
- output sink current up to 800mA and source current up to 100mA
- vertical current sense inputs ground compatible

Figure 41 : Block Diagram



IV.2 - INPUT AMPLIFIER AND RECTIFIER

The input circuitry (Figure 42) is designed for a common mode range up to 12V.

The voltage drop on R1 gives on I_{GND} (Pin 3) :

$$V_{R1} = R1 \cdot I_{REF}$$

The operational amplifier OP regulates the current through R2, thus :

$$I_{R2} = (V_{R1} - V_{IN}) / R2 = (R1 \cdot I_{REF} - V_{IN}) / R2$$

For $V_{IN} > 0$, we note the output current of the input amplifier I_N :

$$I_N = I_{REF} - I_{R2} = I_{REF} - (R1 \cdot I_{REF} - V_{IN}) / R2$$

For $V_{IN} < 0$, we note the output current of the input amplifier I_P :

$$I_P = I_{R2} - I_{REF} = (R1 \cdot I_{REF} - V_{IN}) /R2 - I_{REF}$$

The rectifier is formed by Q2, Q3 and Q4. For $V_{IN} > 0$, I_N flows through Q2 to the rectifier output, thus $I_R = I_N$.

For $V_{IN} < 0$, I_P flows through Q3 from V_S into the output of the input amplifier. Q4 reflects the I_P current, thus the rectifier output currrent will be $I_R = I_{PM} = I_P$.

If the sign convention of I_R is considered, we have :

$$I_R = \left| \frac{(R1 \cdot I_{REF} - V_{IN})}{R} - I_{REF} \right| = \left| I_{REF}\left(\frac{R1}{R2} - 1\right) + \frac{V_{IN}}{R2} \right|$$

In our case, R1 = R2 = 10kΩ and I_{REF} = 120µA

Thus, $I_R = \left| \frac{V_{IN}}{R2} \right|$

If V_{IN} is a symmetrical saw-tooth with GND as the average value and 1.6 $V_{peak\text{-}to\text{-}peak}$, the rectified peak current will be :

$$I_{RP} = \frac{0.8}{10 \cdot 10^{-3}} = 80\mu A$$

IV.3 - VERTICAL CLAMPING

To avoid the parasitic parabola during the vertical flyback time a vertical clamp circuit was used.

The vertical clamping principle is presented in Figure 43.

The rectified sawtooth current I_R Flows through D2 to the output.

When V goes over V_S, Q1 switches off and Q2 on. I_{REF} flows now through D1 to the output and I_R through Q2 to the ground. $I_{RC} = I_{REF}$ is now the clamped value of the output current.

IV.4 - REFERENCE AND STARTING CIRCUIT

Figure 44 presents the complete voltage and current reference circuitry.

The reference current is $I_{REF} = \frac{8.2V}{100k\Omega} = 82\mu A$

To guarantee the start of the device, it is necessary to choose the value of the resistor R5 in order to have a minimum current of 56µA.

Figure 42 : Input and Rectifier Principle Diagram

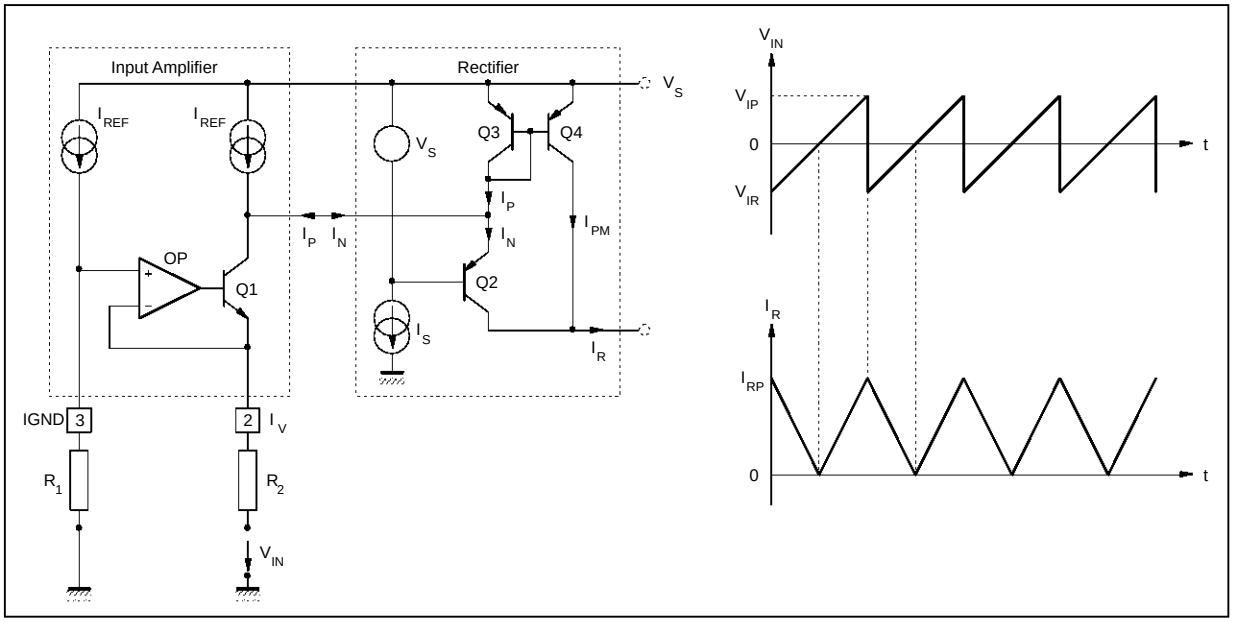


Figure 43 : Vertical Clamping Principle Diagram

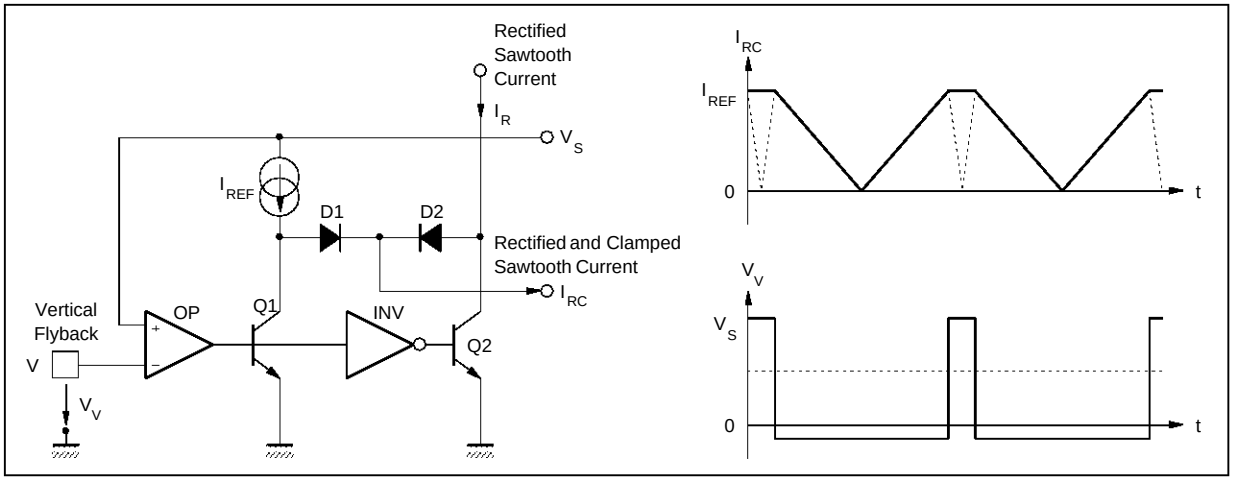
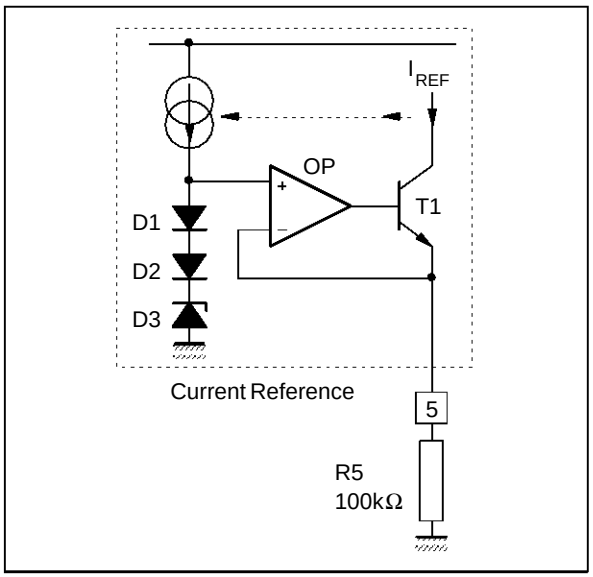


Figure 44 : Reference and Starting Circuit



IV.5 - PARABOLA GENERATOR

Figure 45 presents the simplified circuit diagram of the parabola generator.

The parabolic behaviour of the parabola output current is obtained via piecewise linear approximation.
Two external pins permit an external adjustment of the parabola shape (these pins can be connected to ground or to resistors).

The parabolic output current on Pin 12 Produces a corresponding voltage drop across an external resistor between Pin 12 and ground.

As it can be seen in Figure 46 the parabola can be corrected in the following limits :

V_{C5}/V_C = K5 = 1.07 with Pin 5 to GND
V_{C4}/V_C = K4 = 1.17 with Pins 4 and 5 to GND

An application specific correction can be thus obtained for various picture tube types.

IV.6 - PULSE-WIDTH MODULATOR AND OUTPUT

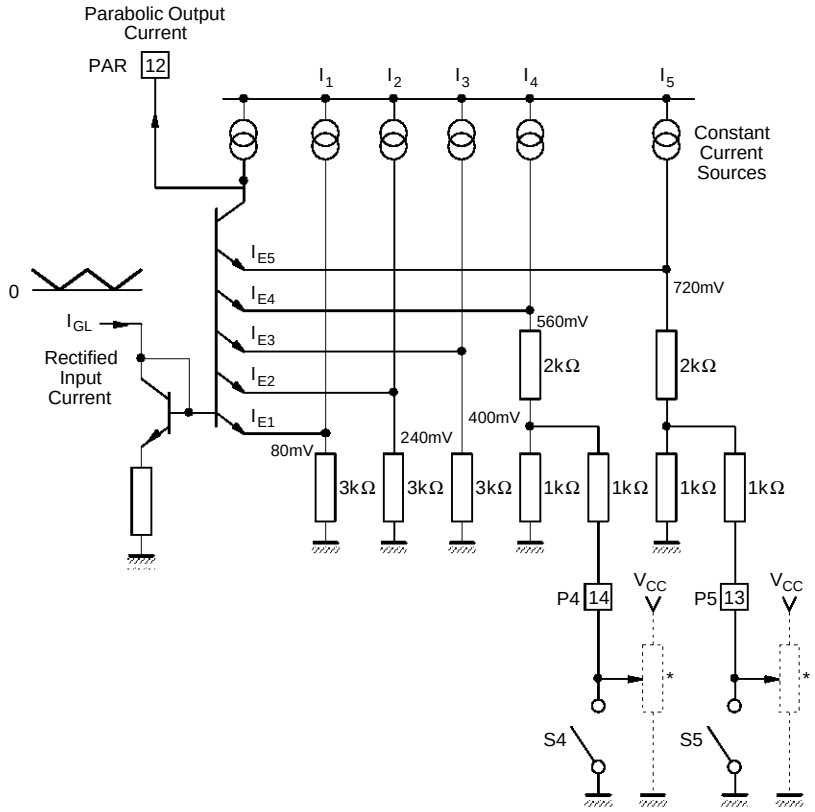
The simplified diagram of the pulse-width modulator and output is presented in Figure 47.

The non-inverting input of the comparator (Pin 11) is connected to a horizontal saw-tooth voltage. An external capacitor connected on Pin 11 is charged during the flyback time and then discharged by the internal current source generating the saw-tooth voltage.

Due to the linear saw-tooth voltage on Pin 11, the comparator works as a pulse-width modulator. The output of this comparator controls the output stage. If the output of the comparator is high, Q67 and Q64 are saturated. The Darlington output configuration Q65/Q66 is switched off. Q62 acts together with R53 as a current source, biasing the current mirror Q58/Q59. The transistor Q60 is switched on.

If the output of the comparator becomes low, Q64 and Q67 are switched off. The current through D58/Q59 disappears and Q60 is switched off. Synchronously the Darlington stage Q65/Q66 is saturated. In order to achieve a fast commutation, an active discharging of the Q60 base charge is provided with the aid of Q63.

Figure 45 : Parabola Generation



Note : * It is possible to replace the switches S4 and S5 by this configuration in order to have a continuous shape variations.

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Figure 46 : Parabola Correction

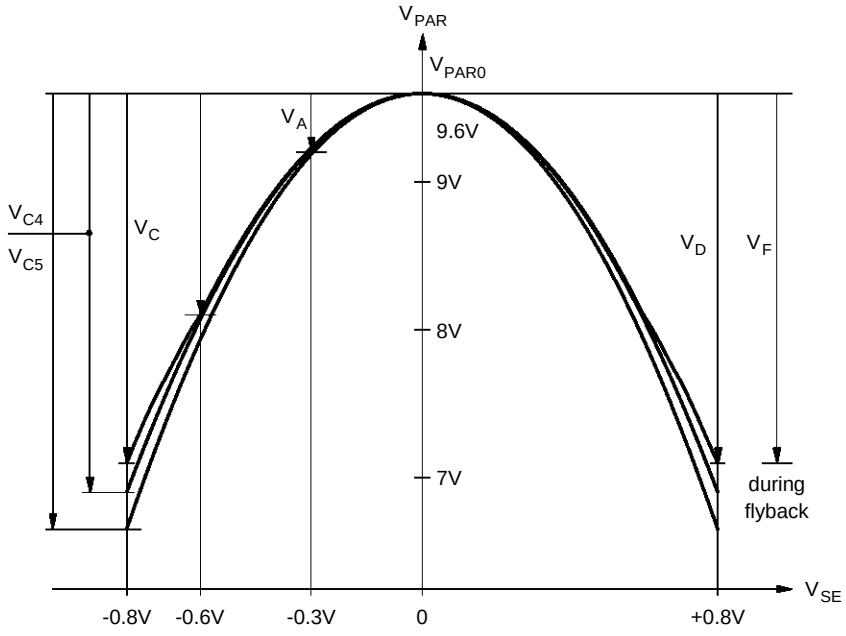

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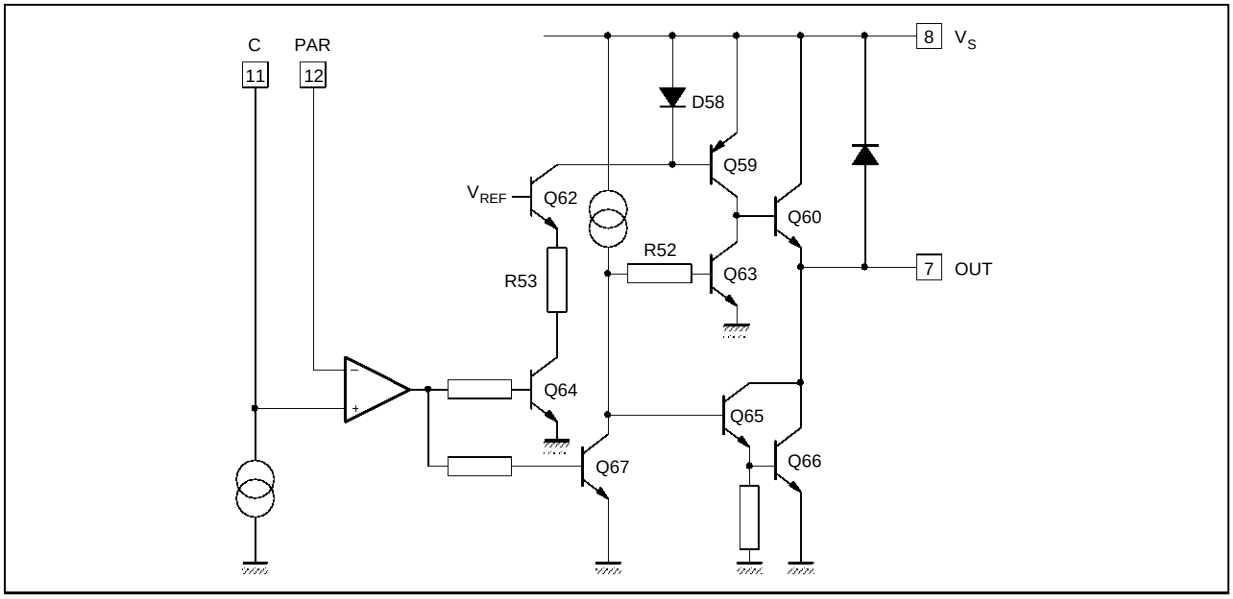
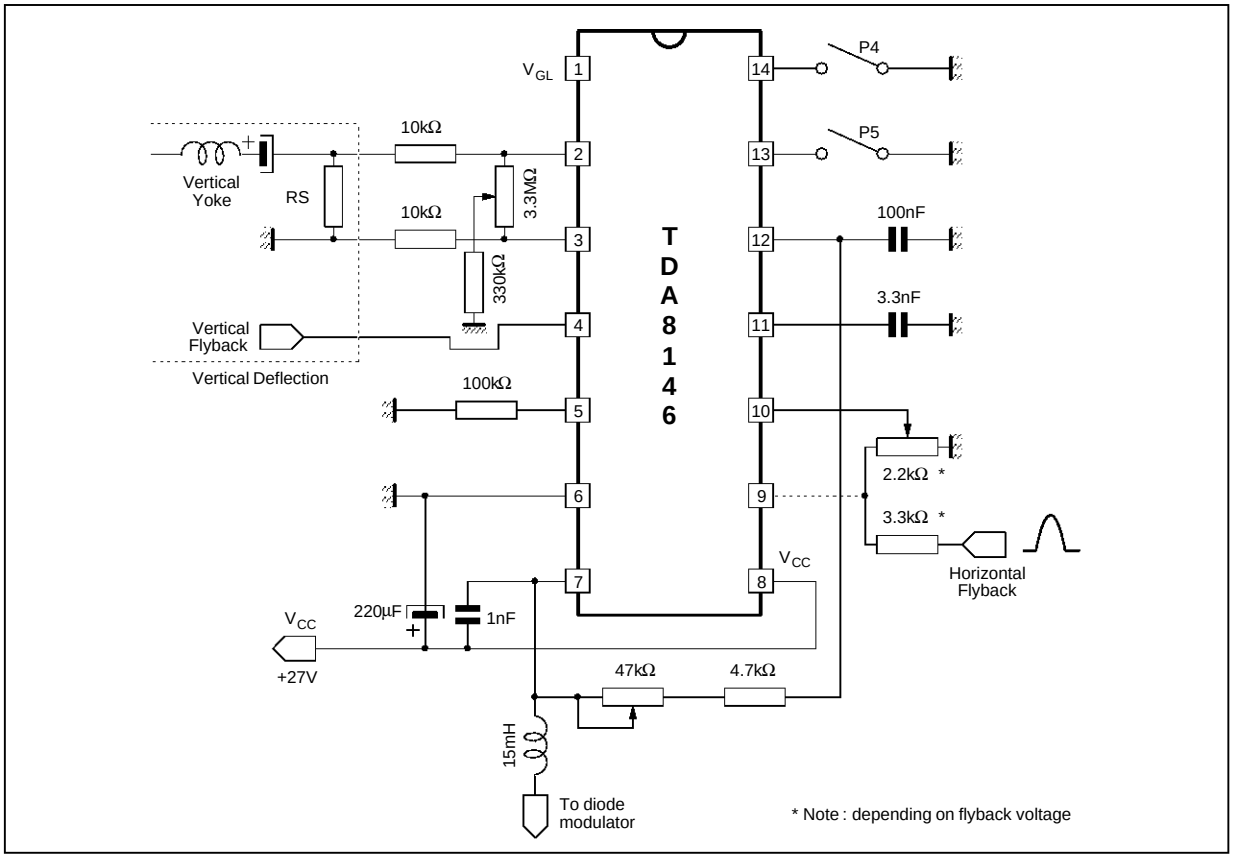
Figure 47 : Pulse-width Modulator and Output



IV.7 - APPLICATION

An application diagram is presented in Figure 48. The internal Zener configuration on Pin 9 can be useful in certain application.

Figure 48 : Application Diagram

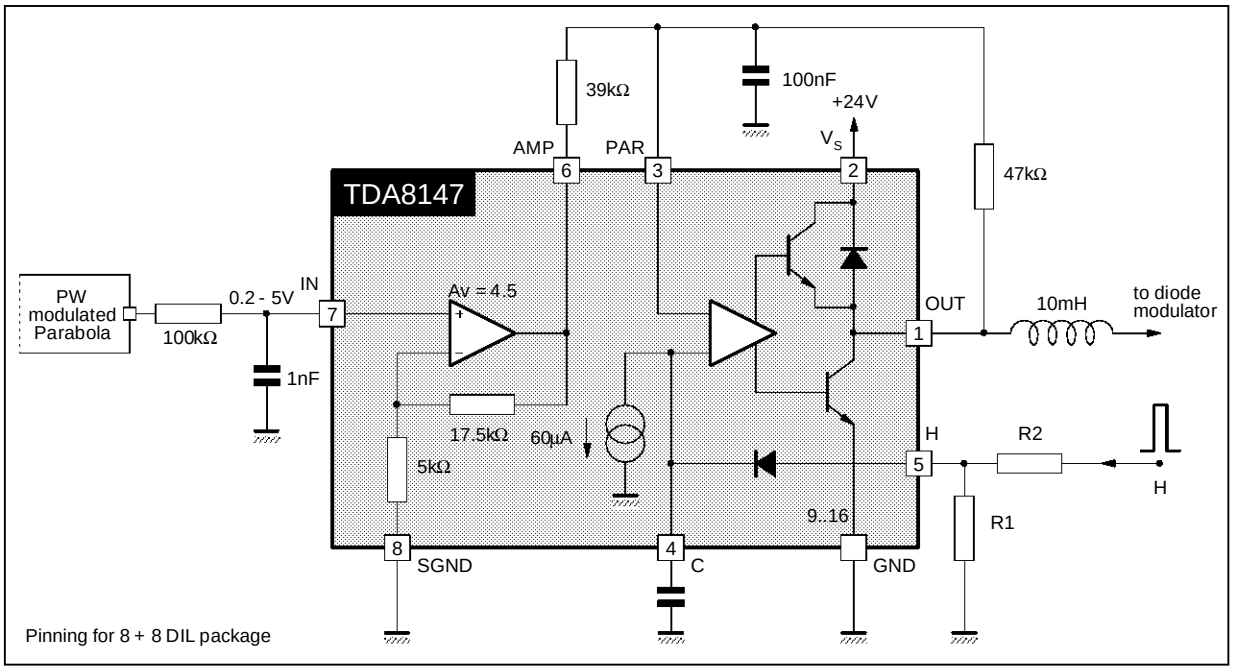


V - TDA8147 GENERAL DESCRIPTION

V.1 - INTRODUCTION

The TDA8147 was designed as an interface IC between the digital circuitry and the diode modulator in digital chassis. The complete block diagram is shown in Figure 49.

Figure 49 : TDA8147 Block Diagram



V.2 - INPUT AMPLIFIER

The pulse-width modulator of the TDA8147 is working with input voltages from 1V to 23V. To have the same range for the parabola voltage an input amplifier is necessary. Digital TV sets deliver an analog parabola or a PWM-signal with small amplitude (2V to 3V).
An additional signal ground (SGND Pin) separates the digital ground from the deflection circuit ground.

The internal feedback loop of the amplifier gives a voltage gain $A_V = \frac{17.5}{5} + 1 = 4.5$ (see Figure 50)

V.3 - VOLTAGE REFERENCE AND STARTING CIRCUIT

The voltage reference and starting circuit have the same configuration as for the TDA8146 (see paragraph IV.4).

V.4 - PWM MODULATOR AND OUTPUT

The PWM modulator (Figure 51) has the same configuration as for the TDA8146. So see paragraph IV.6 for explanation.

V.5 - APPLICATION

A Standard application diagram is given in Figure 51.

Since all the adjustment of the parabola are made by the digital processor, only the feedback loop of the PWM modulator must be carefully designed. The TDA8147 is well-suited for new TV concepts with 32kHz line frequency.

Figure 50 : Input Amplifier

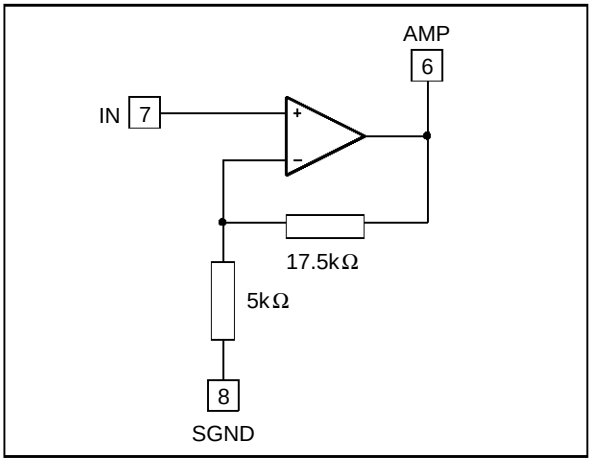


Figure 51 : Application Diagram